ABSTRACT

Double Tail Comparator

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THEORY:

Comparator is the vital building block of analog to digital converter. The need for energy efficient and high speed analog -to-digital converters is necessary for the use of dynamic regenerative comparators to improve speed and efficiency of power. Fast ADCs, such as flash ADCs, requires an energy efficient comparator with small chip area.The sub threshold leakage of transistors has usually been small in the off state,as gate voltage is below threshold.The leakage from all sources has increased as the technology scales down. But as voltages have been scaled down with transistor size, sub threshold leakage has become a considerable factor.This work involves the implementation of an energy efficient double tail comparator with low sub-threshold leakage in eSim.

The circuit mainly operates in two phases, reset phase and decision making phase.In the reset-phase, when Clock=0, p0 & p1 are cut-off and P1 and P2 are on so that the two transistors N1 and N2 will be on and pulls the two output nodes out1 and out2 to zero potential.In decision-phase, when Clock=positive power supply(VDD), the two tail transistors p1 and p0 are on and P1 and P2 are off which turns the two tranistors N1 and N2 off. Consider the case where IN1>IN2, then the transistors N2 will turn on faster so the output of that inverter falls down which turns the intermediate transistor N1 off. Hence, out1 pulls up to VDD. When out1 goes to VDD, the transisto p3 will be off which remains out2 at ground. By using this approach approaches the sub-threshold leakage and hence the total power will be reduced. The simulation results prove the reduction. Here in the differential amplifier inverters are used which are series transistors. Hence, the trans conduc-tance of the total circuit increases which reduces the total delay of the circuit. Hence, by using this CMOS inverter approach the total power and delay can be reduced.

CIRCUIT DIAGRAM :

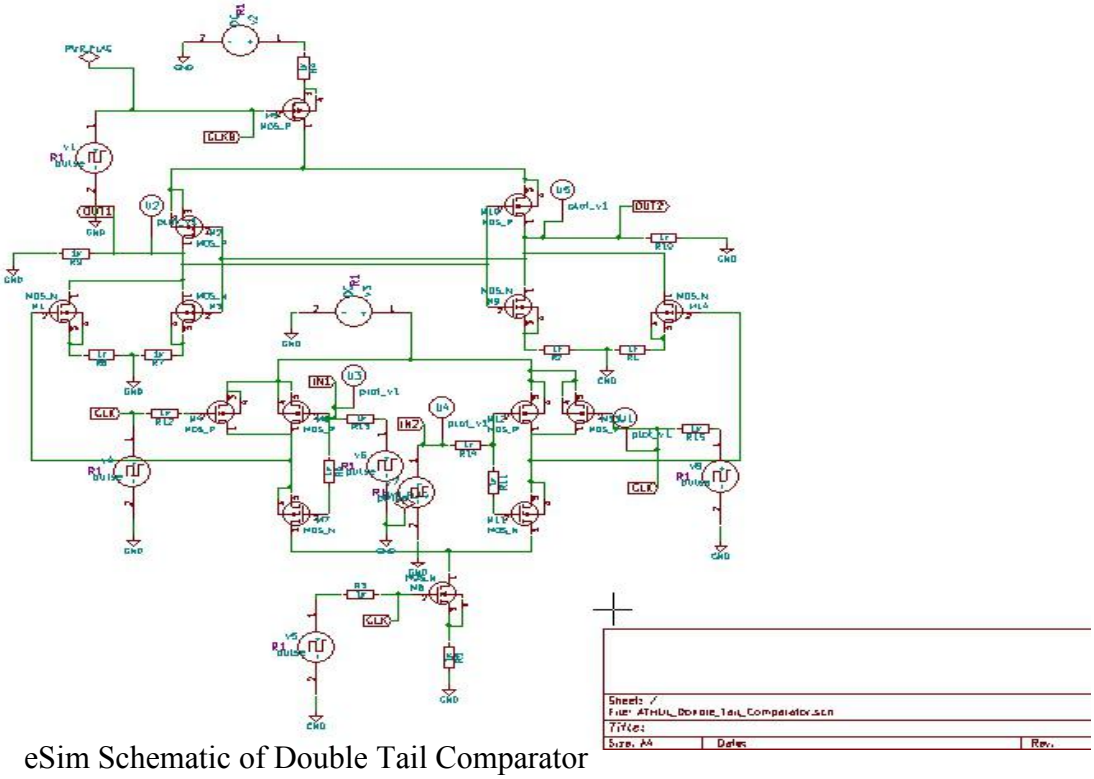
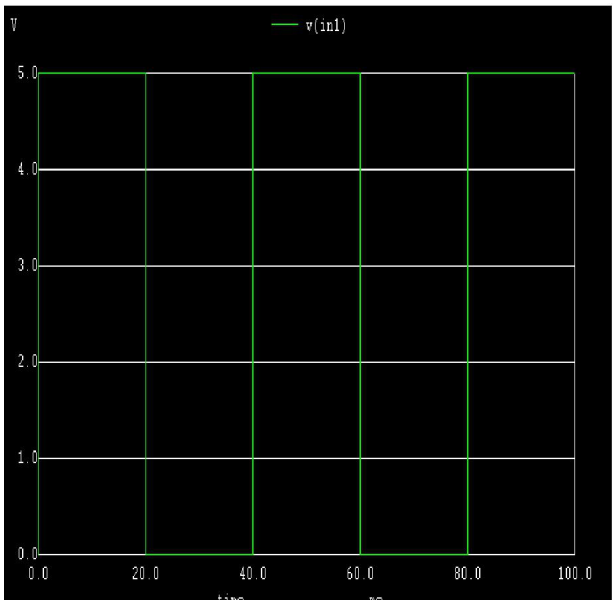


Fig.1 eSim Schematic of Double Tail Comparator

SIMULATION RESULTS

1. Ngspice



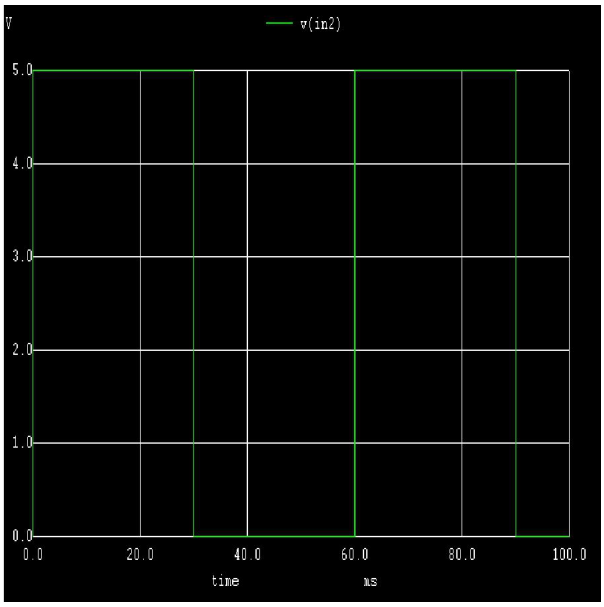


Fig.**2 Input Pulses IN1,IN2** ;

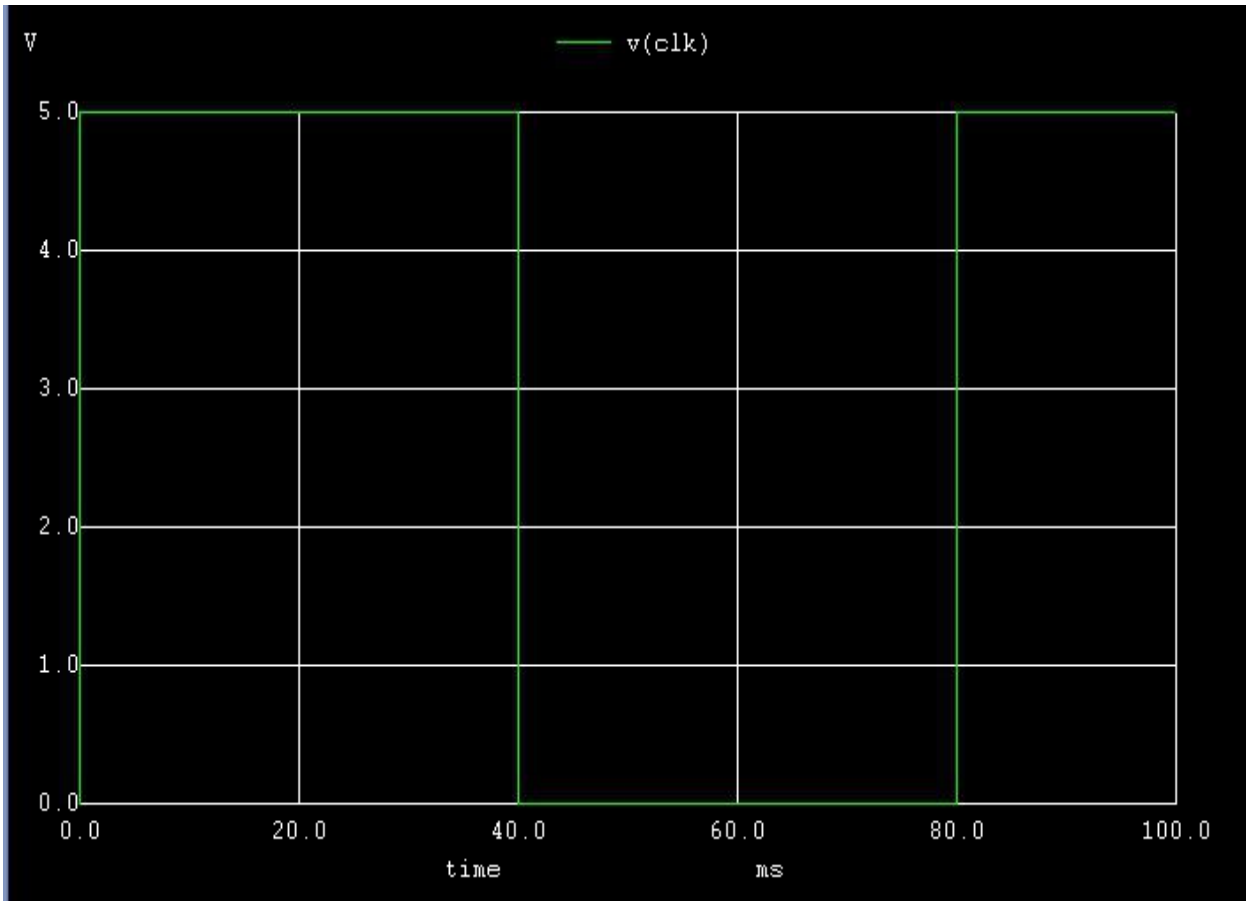
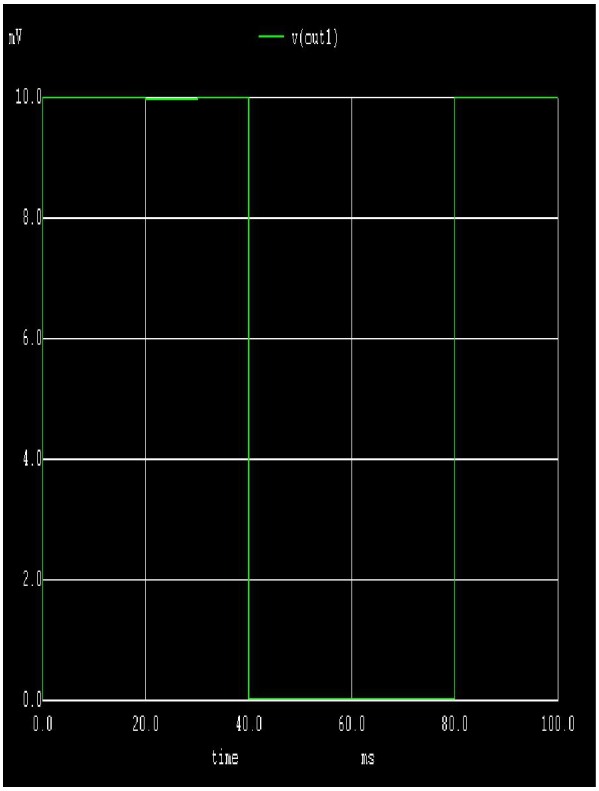


Fig.3 Clock Signal



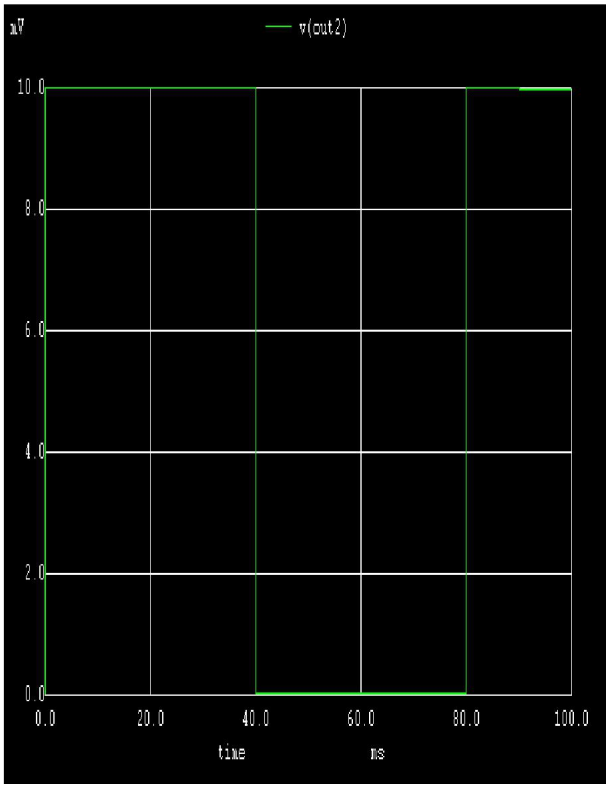


Fig.4 Output pulses

Python

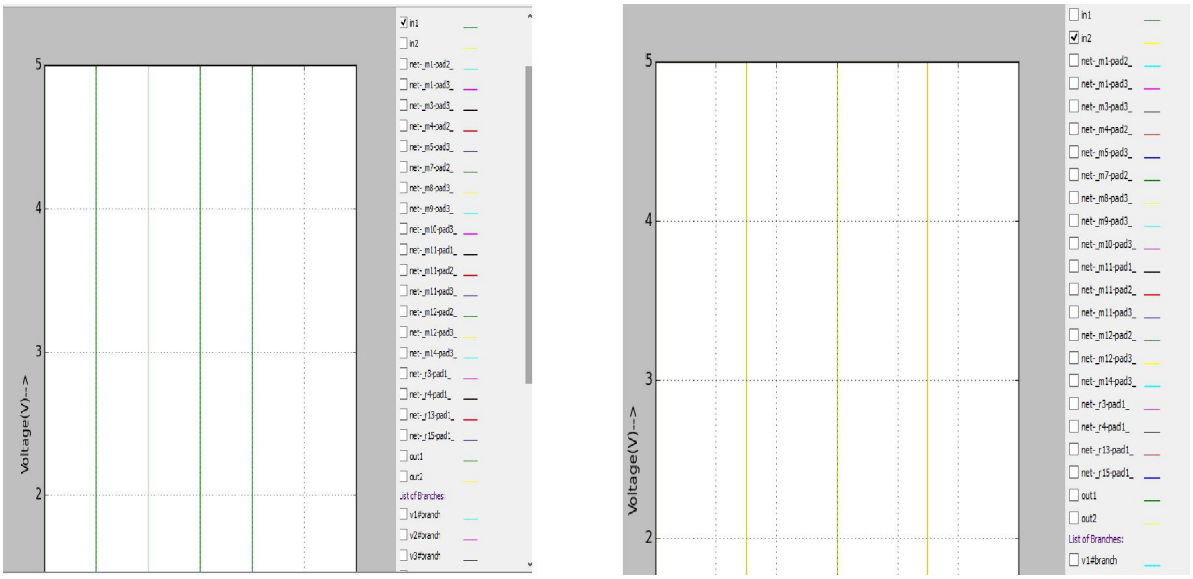


Fig.5 Input Pulses

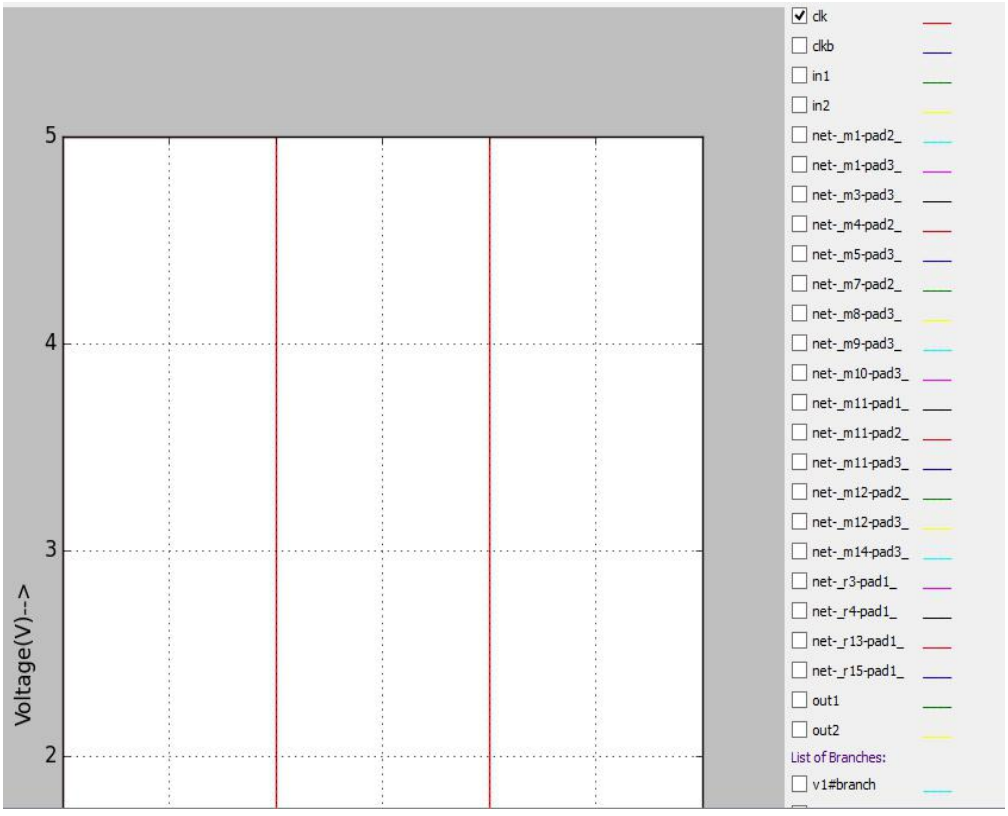


Fig 6 Clock signal

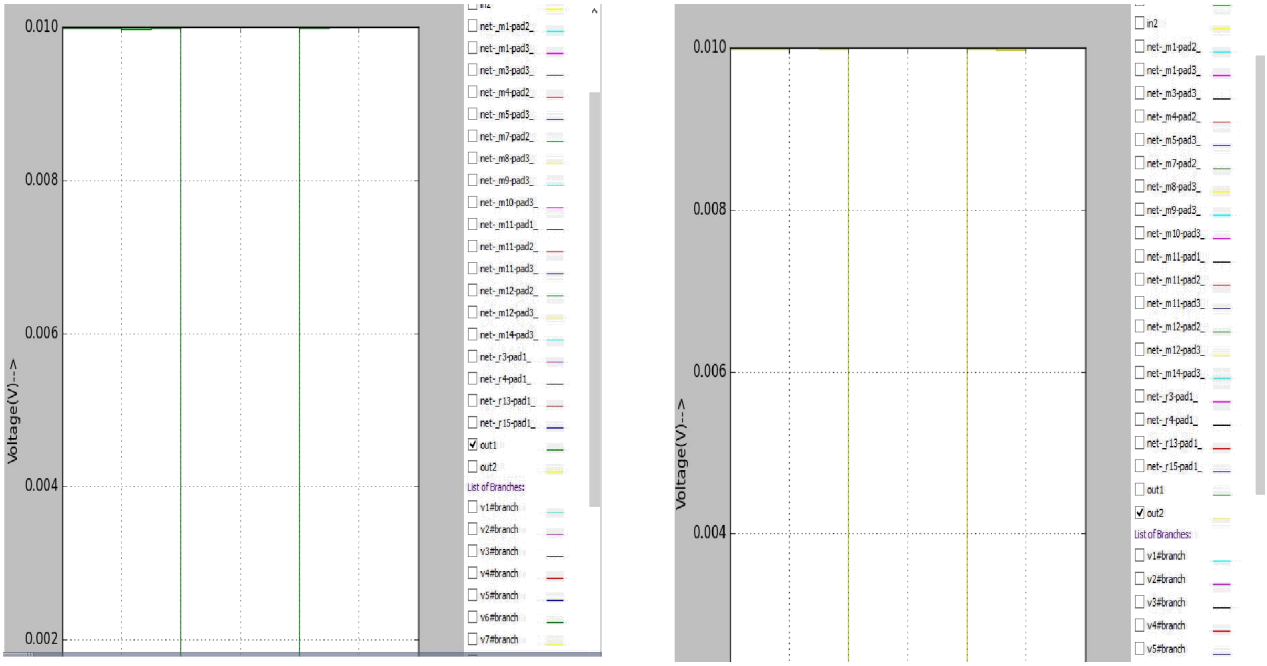


Fig.7 Output pulses

REFERENCES:

http://ieeexplore.ieee.org/document/8186675/