CASCADED BIPOLAR JUNCTION TRANSISTOR AMPLIFIER

BY:

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THEORY:

A multistage cascade where each stage is separately biased and coupled to adjacent stages via DC blocking capacitors. Inserting coupling capacitors between stages blocks the DC operating bias level of one stage from affecting the DC operating point of the next. This solves many of the limitations called loading effect. However, the resulting overall amplifier can no longer respond to DC, or very low frequency, inputs.

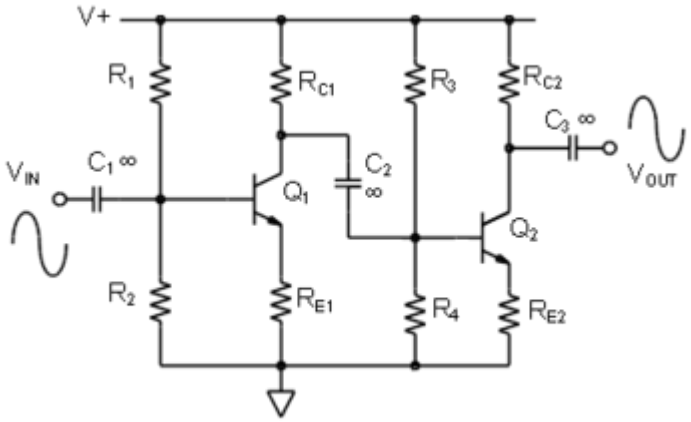


Figure 10.1.3 AC coupled Common Emitter stages

The infinity symbol next to coupling capacitors C_1 C_2 and C_3 is used to indicate that the unspecified capacitance is large enough at the specified signal frequency to have a negligible reactance and can be treated as an AC short-circuit. It is also useful to note at this point that the method of including capacitors across the emitter degeneration resistors R_{E1} and R_{E2} to increase the gain at higher frequencies can be employed in the case of these multistage amplifiers as well as the single stage amplifiers .

DESIGN:

The Cascaded BJT Amplifier is designed for 60Hz and input is given 0.4V

and the output got is 4V.

R1=22K

R2=4.7K

R3=22K

R4=4.7K

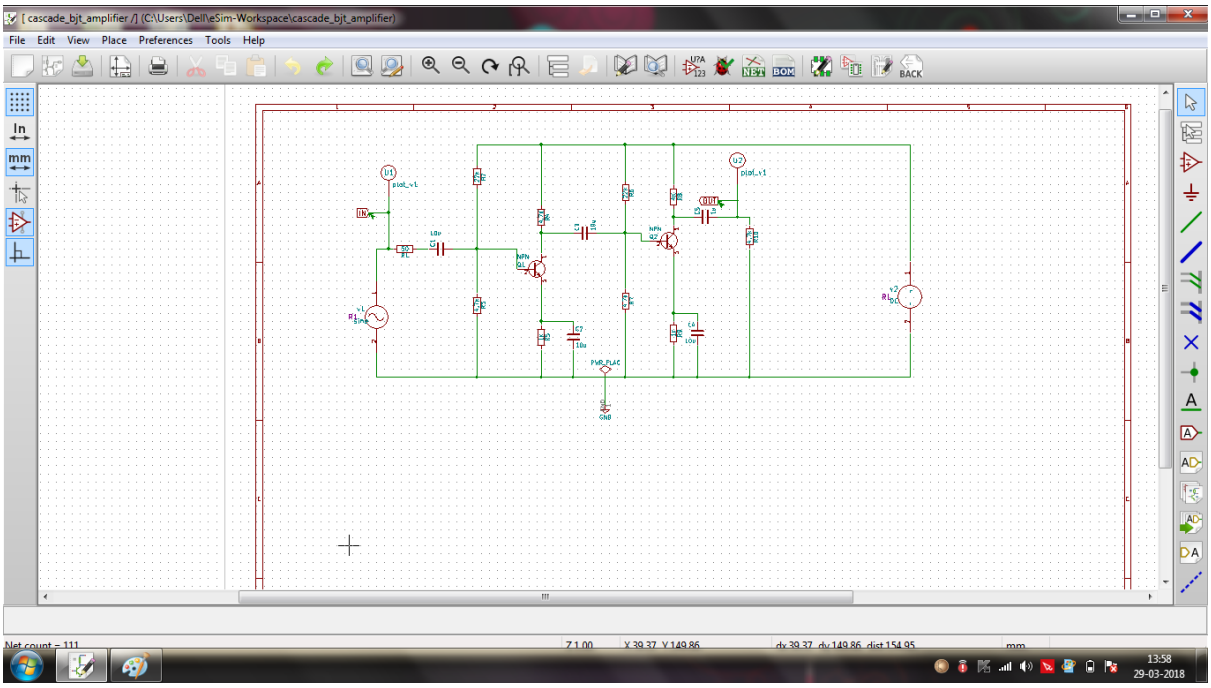
RE1=1k

RE2=1k

RC1=4.7K

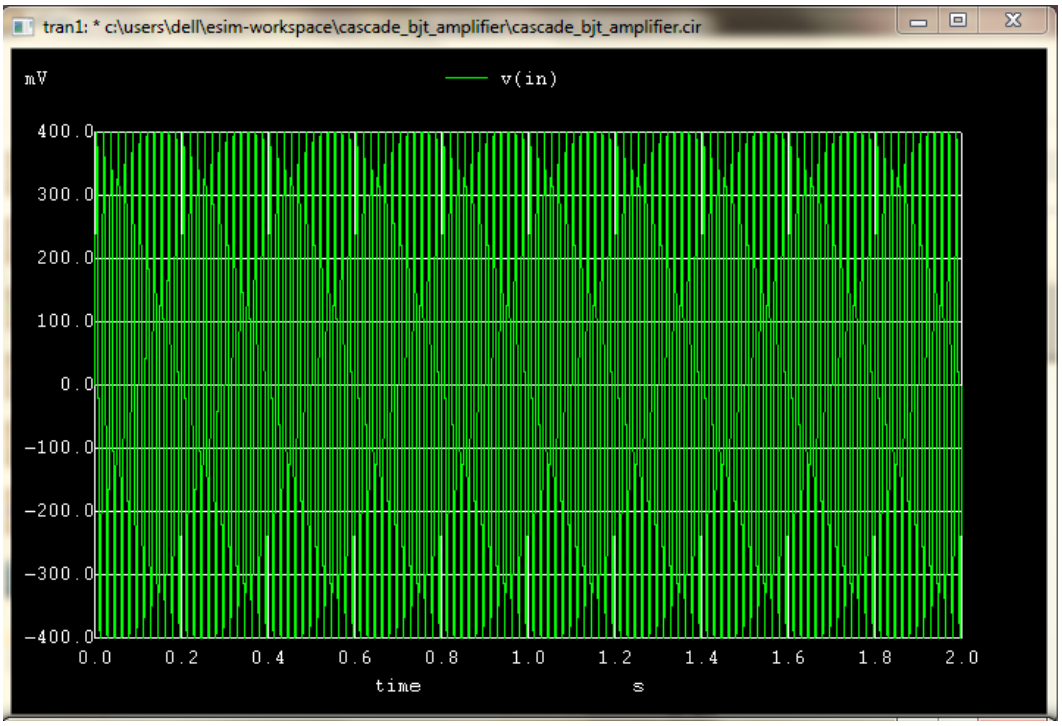
RC2=4K

Design Schematic :

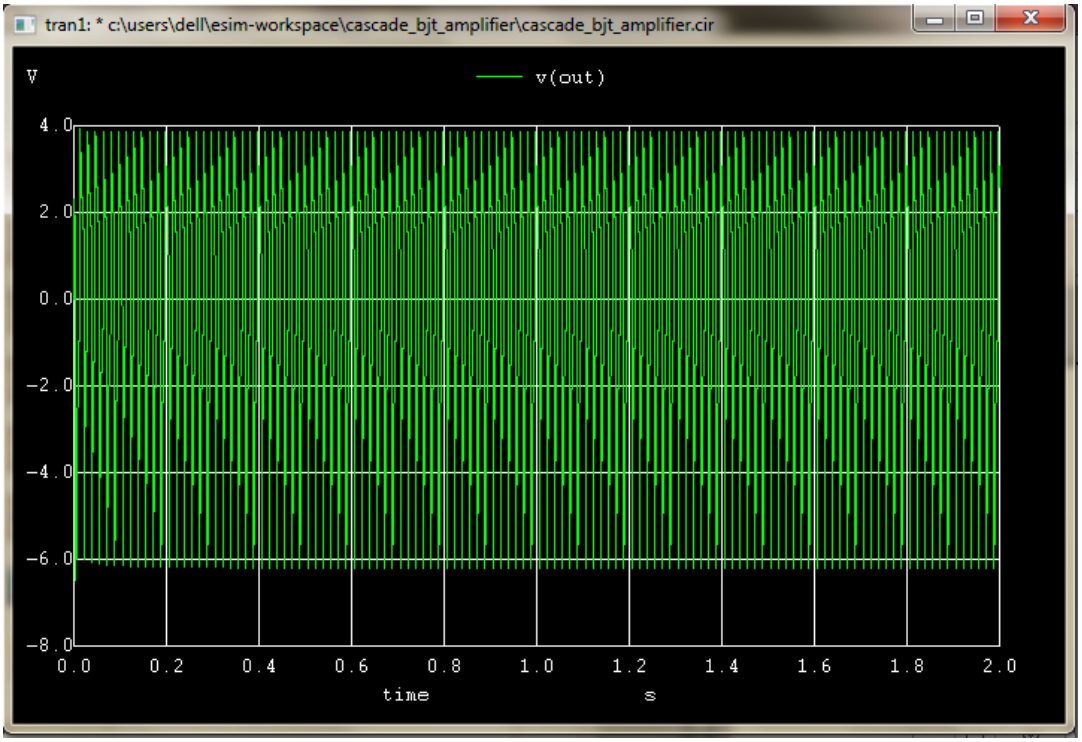


Ngspice Plots:

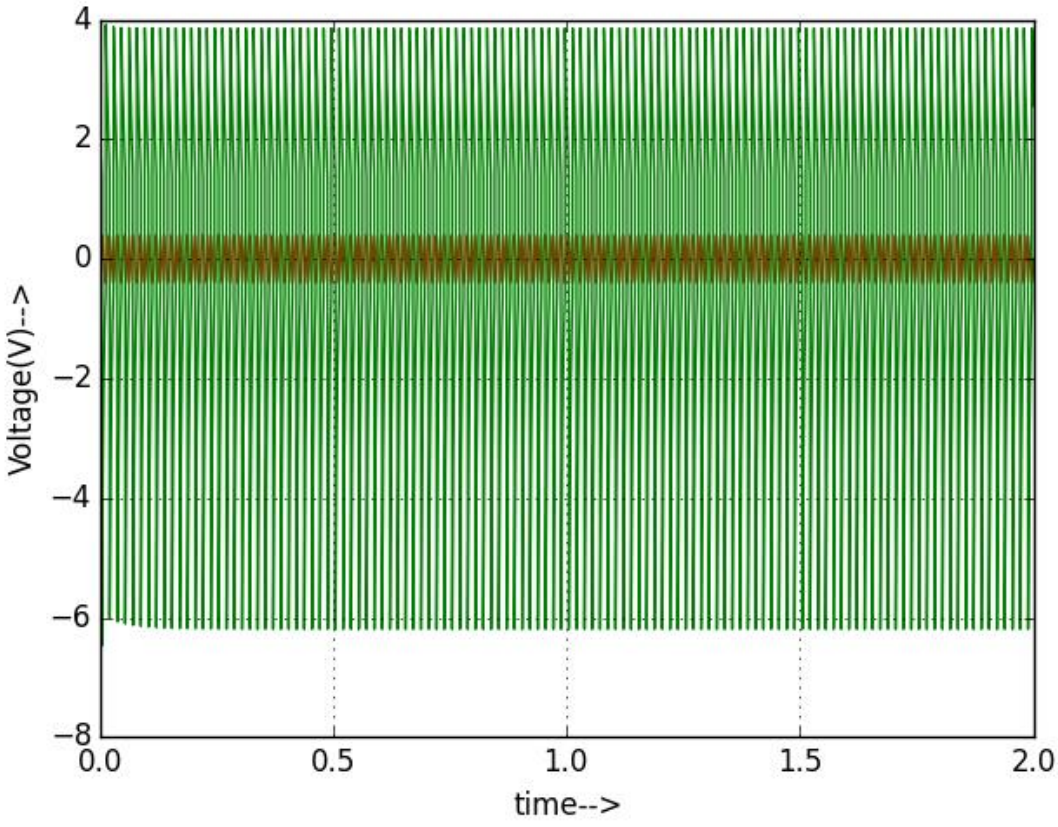
Input plot:



OUTPUT PLOT:



Python plot:



REFERENCE:
https://wiki.analog.com/university/courses/electronics/text/chapter-10