

ABSTRACT

Design and Implementation Voltage Doubler & Tripler Circuit Using Diodes

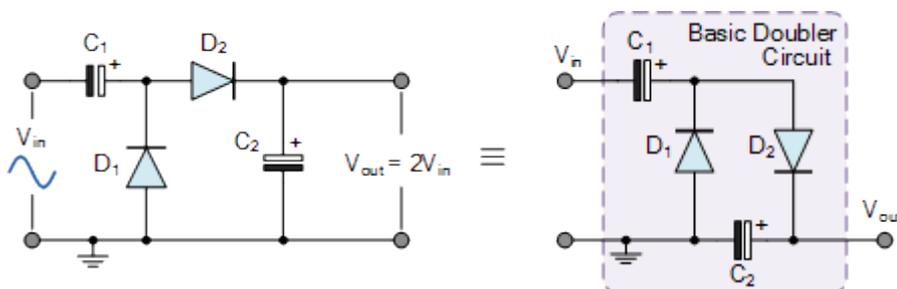
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Theory:

The Voltage Doubler

As its name suggests, a **Voltage Doubler** is a circuit which gives output voltage 2 times of input peak voltage. The circuit consists of only two diodes, two capacitors and an oscillating AC input voltage (a PWM waveform could also be used). This simple diode-capacitor pump circuit gives a DC output voltage equal to the peak-to-peak value of the sinusoidal input. In other words, double the peak voltage value because the diodes and the capacitors work together to effectively double the voltage.

DC Voltage Doubler Circuit



So how does it work. The circuit shows a half wave voltage doubler. During the negative half cycle of the sinusoidal input waveform, diode D1 is forward biased and conducts charging up the pump capacitor, C1 to the peak value of the input voltage, (V_p). Because there is no return path for capacitor C1 to discharge into, it remains fully charged acting as a storage device in series with the voltage supply. At the same time, diode D2 conducts via D1 charging up capacitor, C2.

During the positive half cycle, diode D1 is reverse biased blocking the discharging of C1 while diode D2 is forward biased charging up capacitor C2. But because there is a voltage across capacitor C1 already equal to the peak input voltage, capacitor C2 charges to twice the peak voltage value of the input signal.

In other words, $V(\text{positive peak}) + V(\text{negative peak})$, so on the negative half-cycle, D1 charges C1 to V_p and on the positive half-cycle D2 adds the AC peak voltage to V_p on C1 and transfers it all to C2. The voltage across capacitor, C2 discharges through the load ready for the next half cycle.

Then the voltage across capacitor, C2 can be calculated as: $V_{out} = 2V_p$, (minus of course the voltage drops across the diodes used) where V_p is the peak value of the input voltage. Note that this double output voltage is not instantaneous but increases slowly on each input cycle, eventually settling to $2V_p$.

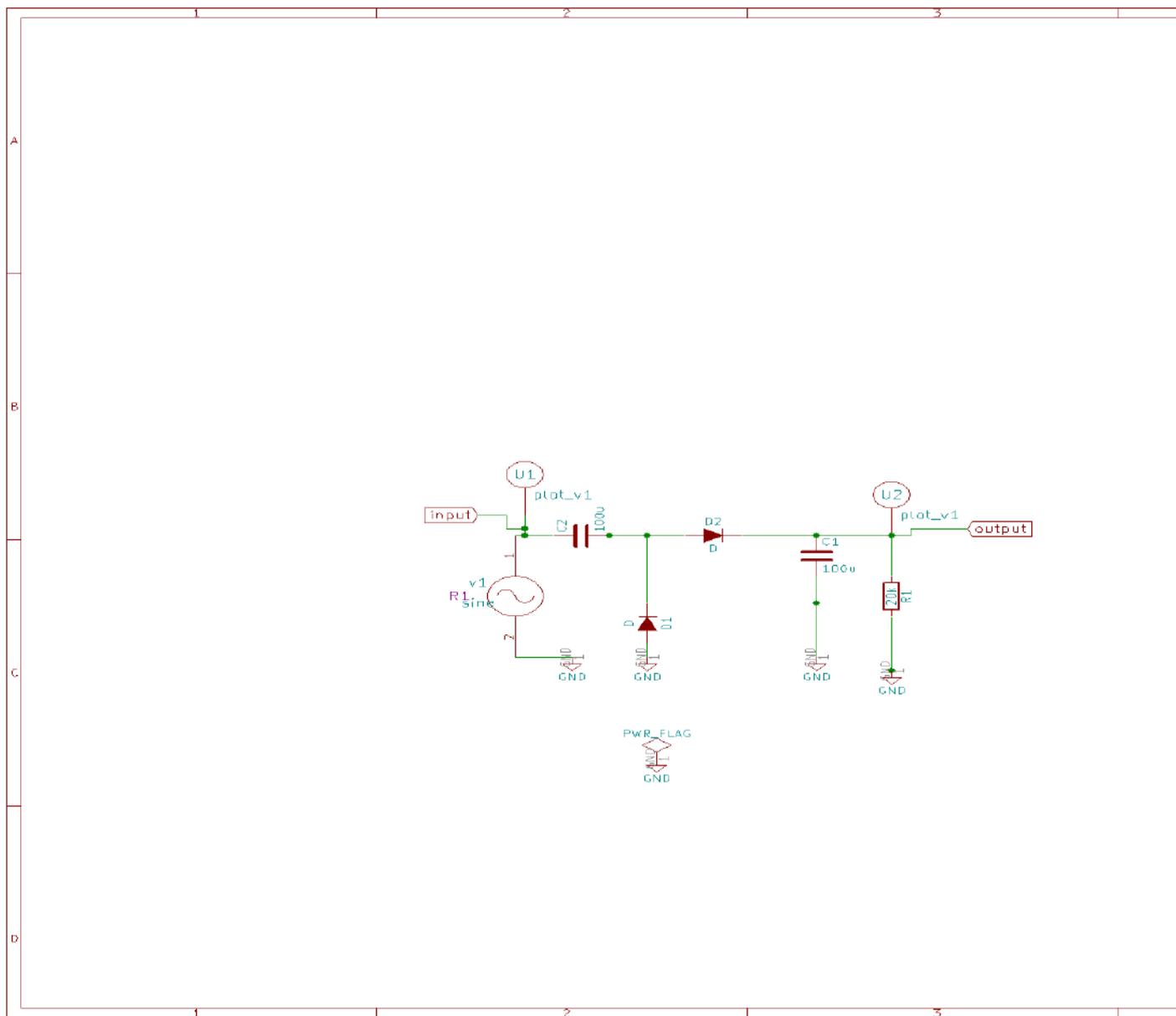
As capacitor C2 only charges up during one half cycle of the input waveform, the resulting output voltage discharged into the load has a ripple frequency equal to the supply frequency, hence the name half wave voltage doubler. The disadvantage of this is that it can be difficult to smooth out this large ripple frequency in

much the same way as for a half wave rectifier circuit. Also, capacitor C2 must have a DC voltage rating at least twice the value of the peak input voltage.

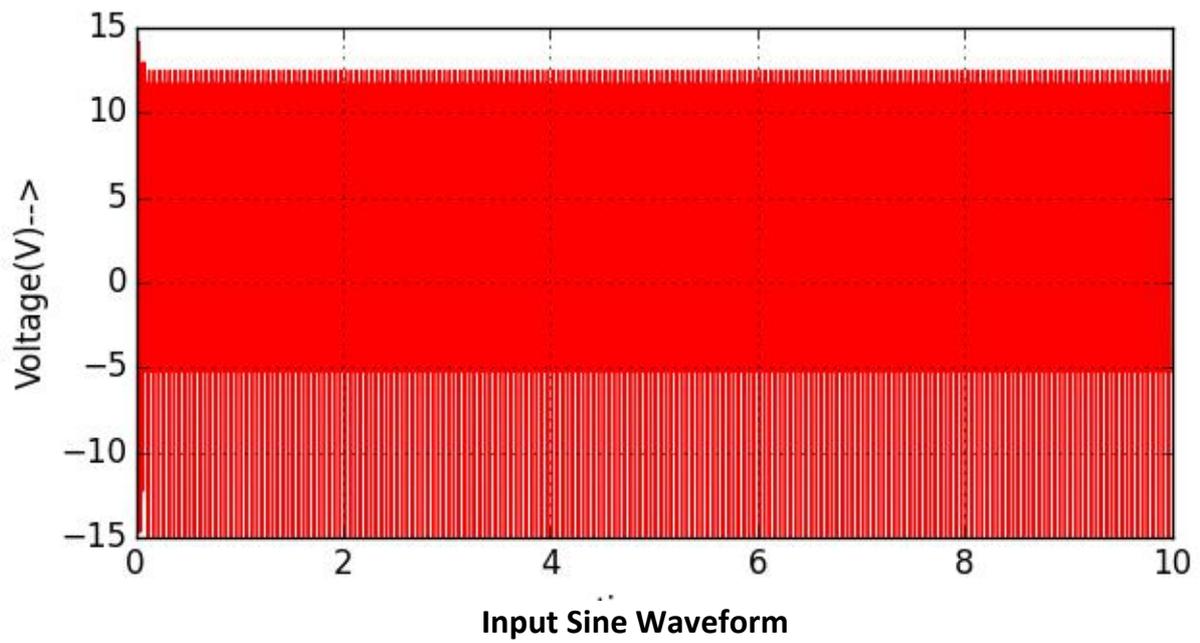
Advantages of Voltage Doubler

- Can replace the expensive and heavy transformers.
- Negative voltage can also be created by reversing the polarity of the connected diodes and capacitors.
- Can increase the voltage multiplication factor by cascading the similar voltage multipliers.

Design:

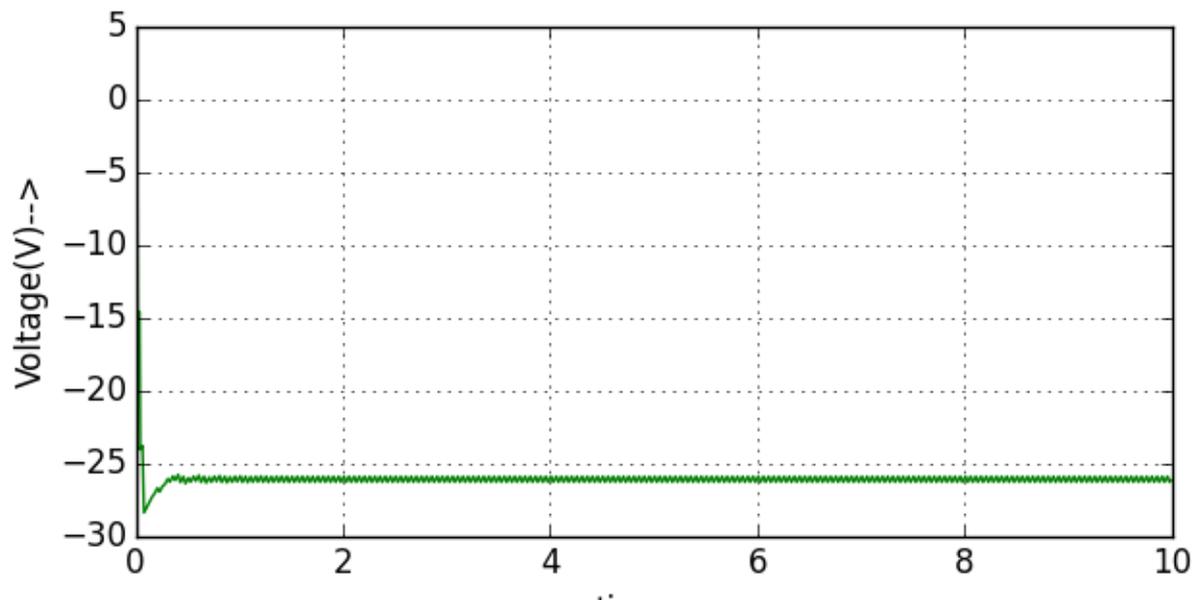


Python plots



Node/Branch	RMS Value
input	10.514

Input RMS Voltage

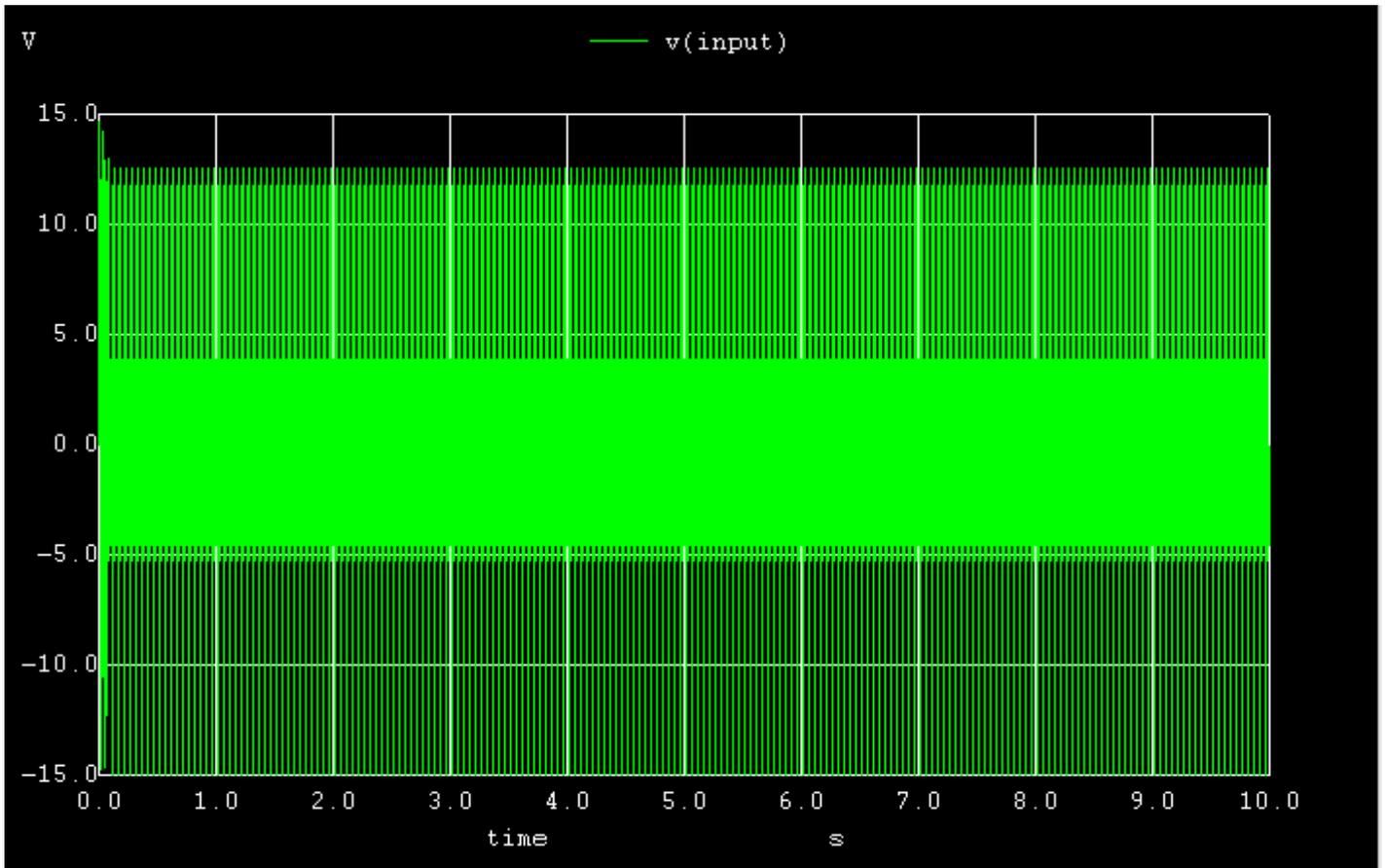


Waveform of Output

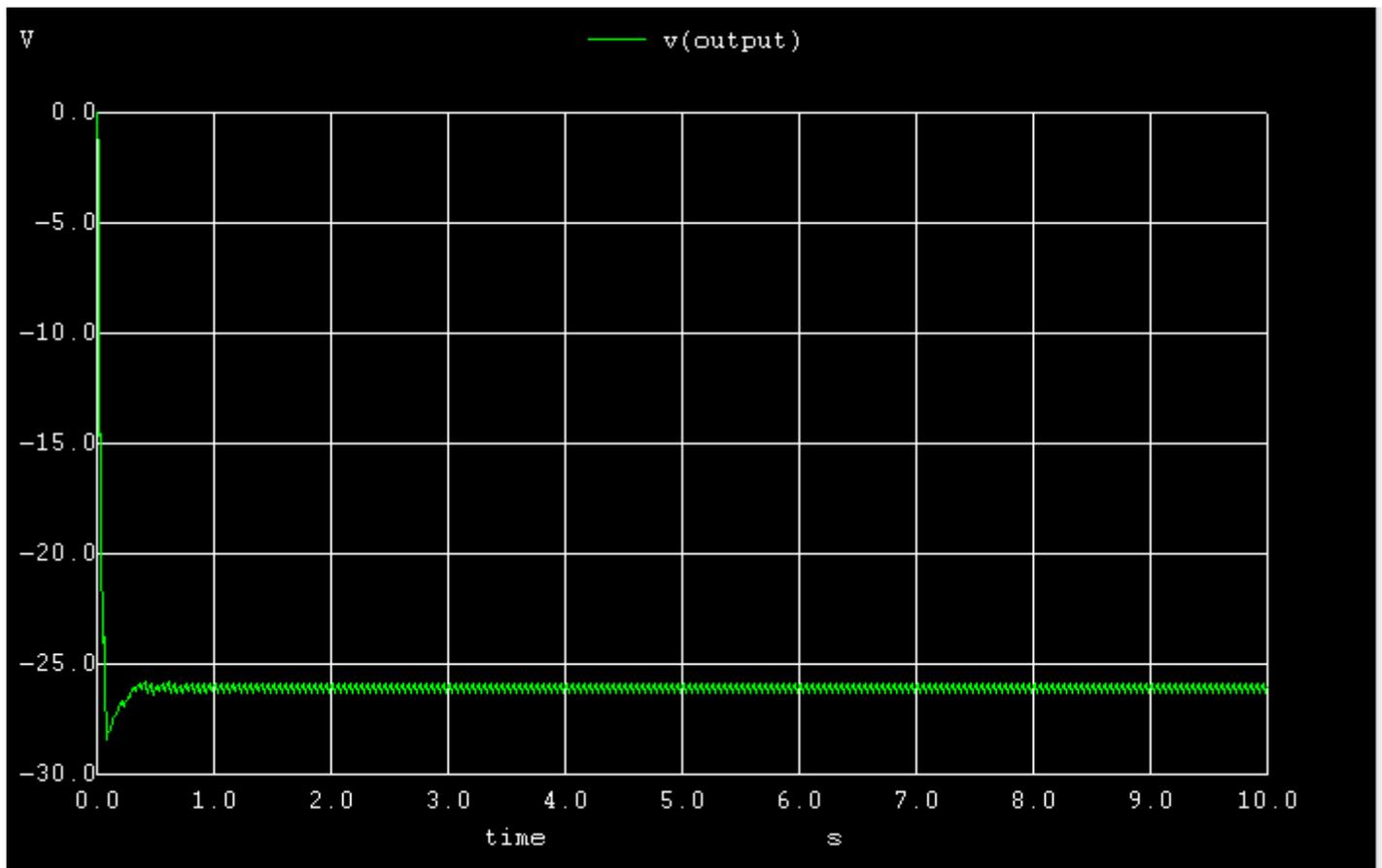
Node/Branch	RMS Value
output	25.662

Output voltage RMS

Ngspice plots:



Input Sine Waveform



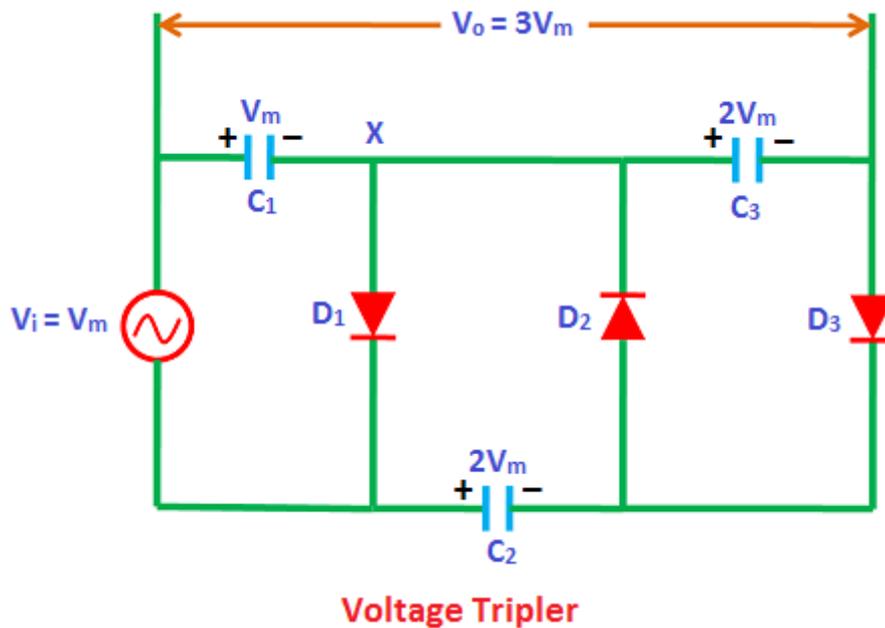
Output Plot of Waveform

The Voltage Tripler

As its name suggests, a Voltage tripler circuit gives a DC output equal to three times the peak voltage value ($3V_p$) of the sinusoidal input signal

During first positive half cycle:

During the first positive half cycle of the input AC signal, the diode D1 is forward biased whereas diodes D2 and D3 are reverse biased. Hence, the diode D1 allows electric current through it. This current will flow to the capacitor C1 and charges it to the peak value of the input voltage i.e. V_m .



During negative half cycle:

During the negative half cycle, diode D_2 is forward biased whereas diodes D_1 and D_3 are reverse biased. Hence, the diode D_2 allows electric current through it. This current will flow to the capacitor C_2 and charges it. The capacitor C_2 is charged to twice the peak voltage of the input signal ($2V_m$). This is because the charge (V_m) stored in the capacitor C_1 is discharged during the negative half cycle.

Therefore, the capacitor C_1 voltage (V_m) and the input voltage (V_m) is added to the capacitor C_2 i.e. Capacitor voltage + input voltage = $V_m + V_m = 2V_m$. As a result, the capacitor C_2 charges to $2V_m$.

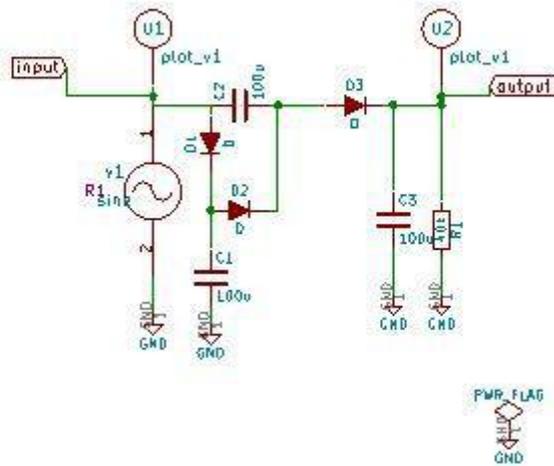
During second positive half cycle:

During the second positive half cycle, the diode D_3 is forward biased whereas diodes D_1 and D_2 are reverse biased. Diode D_1 is reverse biased because the voltage at X is negative due to charged voltage V_m , across C_1 and diode D_2 is reverse biased because of its orientation. As a result, the voltage ($2V_m$) across capacitor C_2 is discharged. This charge will flow to the capacitor C_3 and charges it to the same voltage $2V_m$.

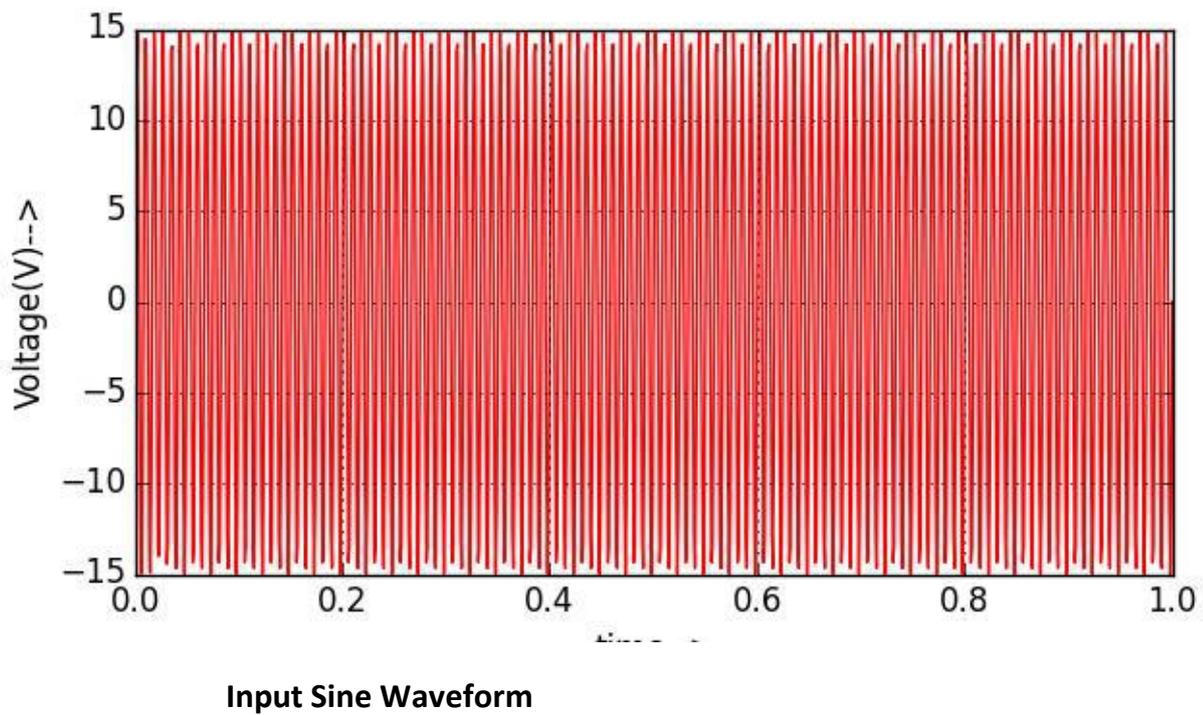
The capacitors C_1 and C_3 are in series and the output voltage is taken across the two series connected capacitors C_1 and C_3 . The voltage across capacitor C_1 is V_m and capacitor C_3 is $2V_m$. So the total output voltage is equal to the sum of capacitor C_1 voltage and capacitor C_3 voltage i.e. $C_1 + C_3 = V_m + 2V_m = 3V_m$.

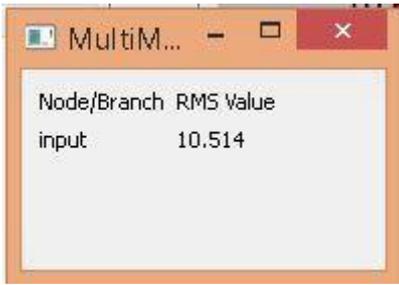
Therefore, the total output voltage obtained in voltage tripler is $3V_m$ which is three times more than the applied input voltage

Design:



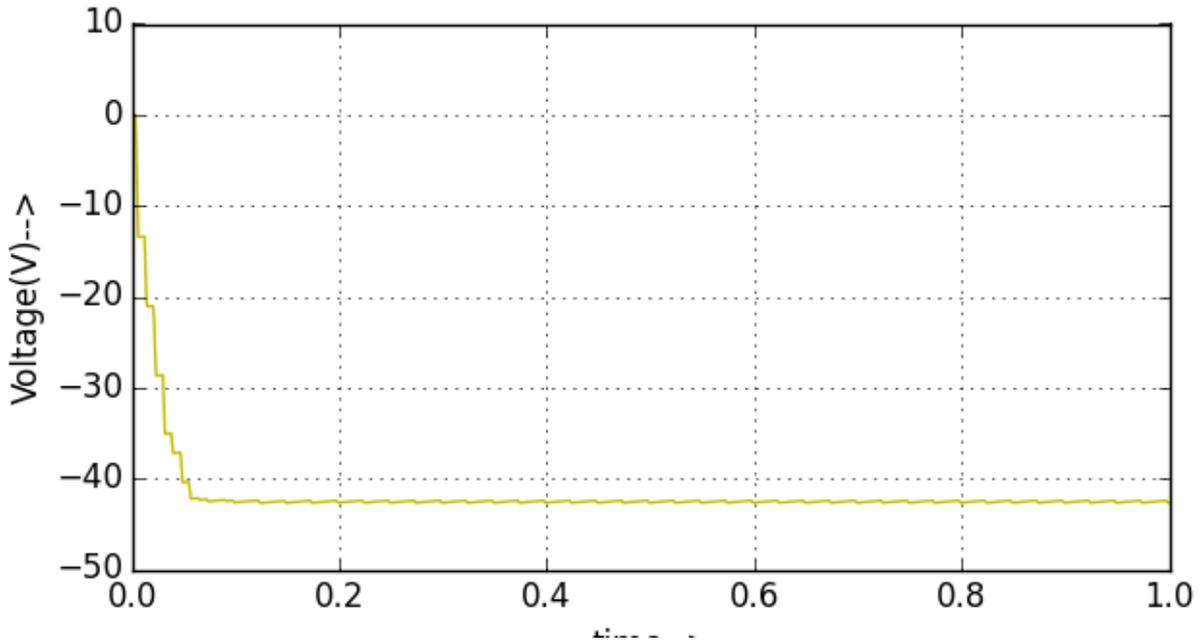
Python plots



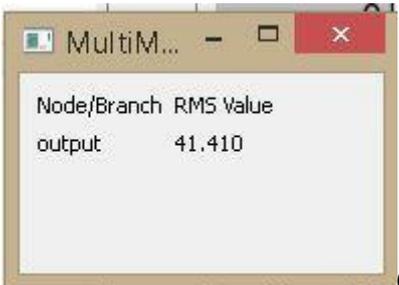


Node/Branch	RMS Value
input	10.514

input RMS Voltage



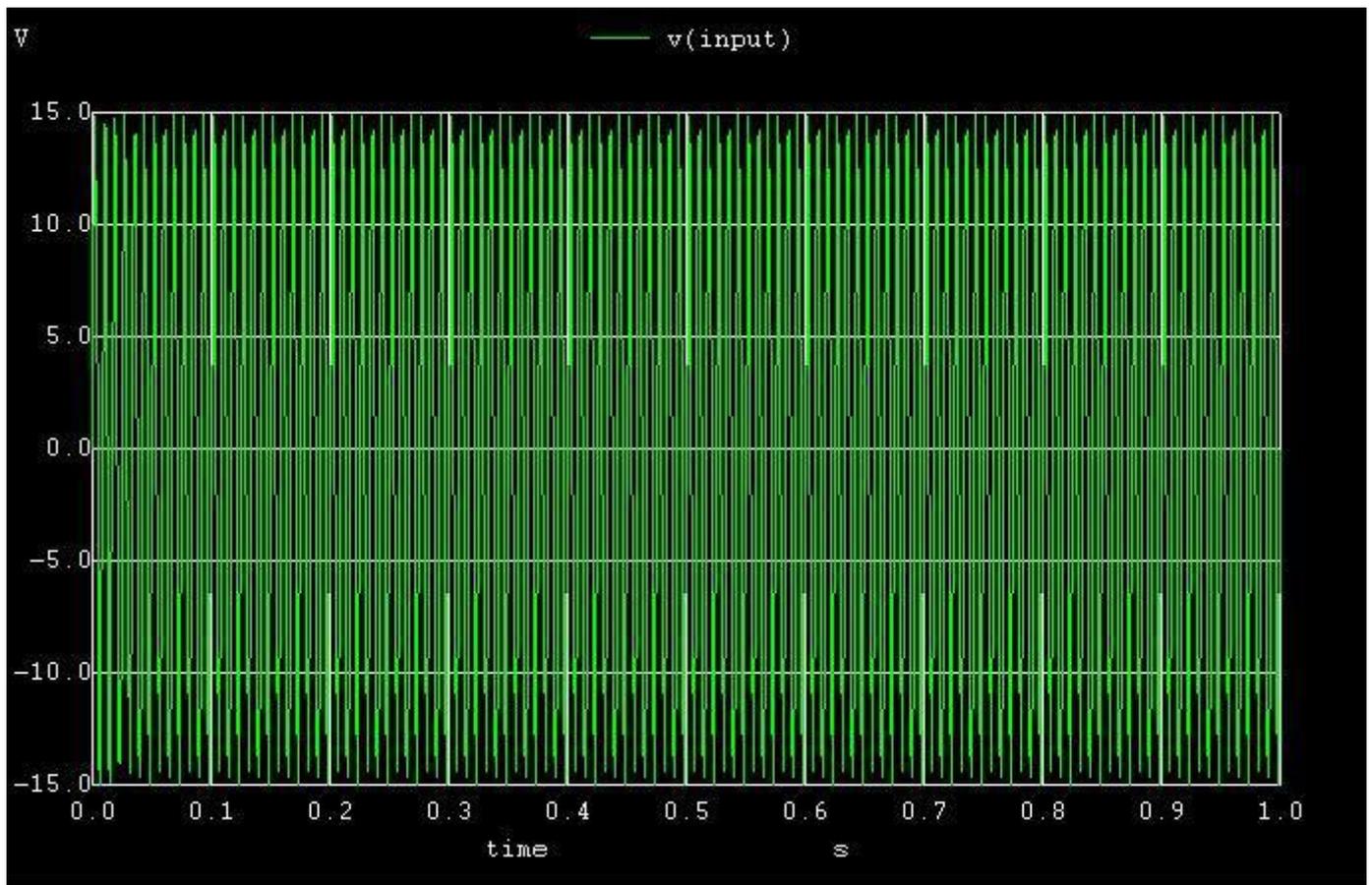
Waveform of Output



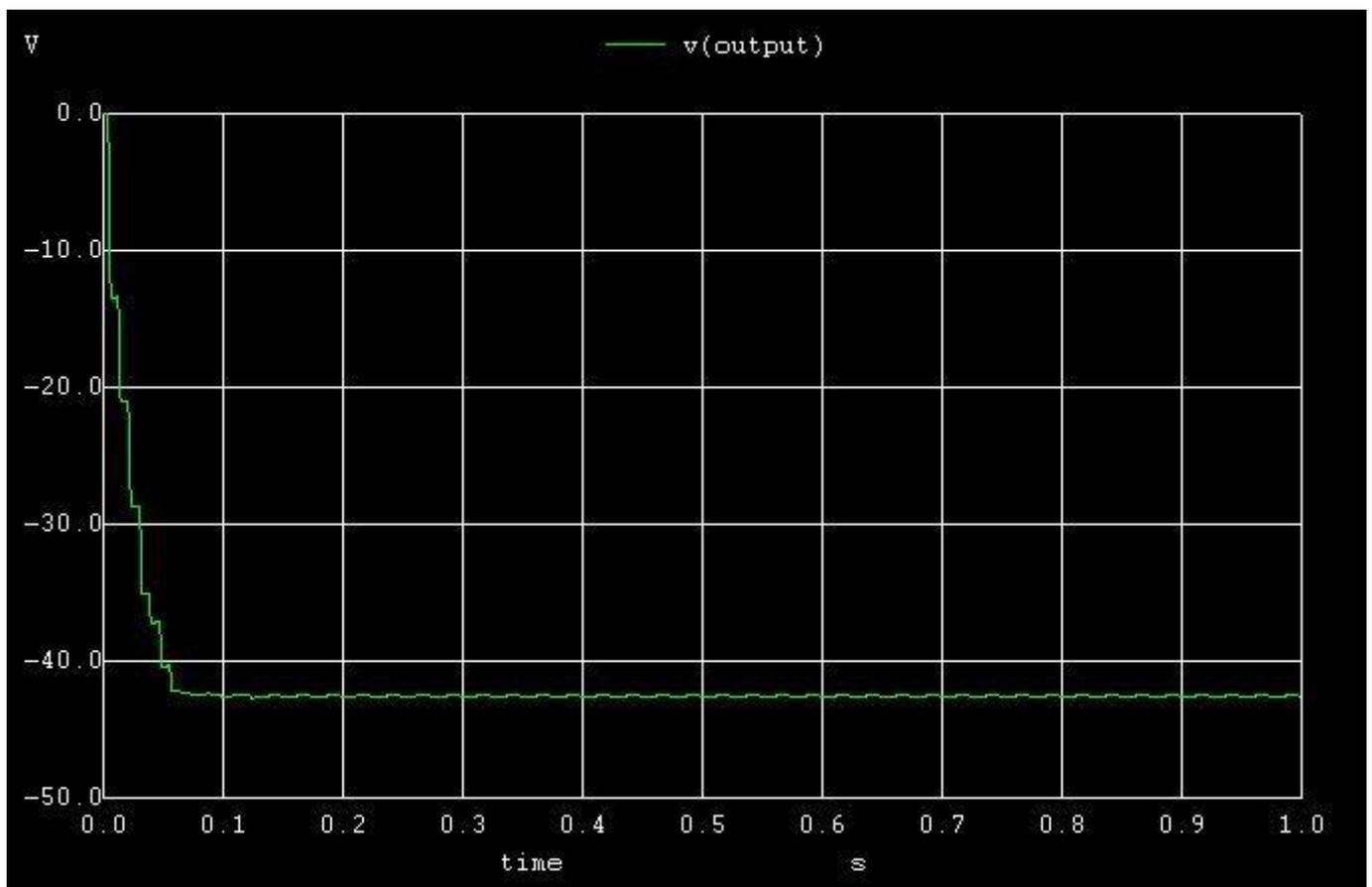
Node/Branch	RMS Value
output	41.410

Output voltage RMS

Ngspice plots:



Input Sine Waveform



Output Plot of Waveform

Reference:

<https://www.electronics-tutorials.ws/blog/voltage-multiplier-circuit.html>