ABSTRACT

Design and Implementation Synchronous Decade Counter

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Theory:

"**Synchronous counter**" is a counter circuit, which created from the series of J-K flip-flops. The clock signal will be given to the clock input of the all J-K flip-flop The output signal, which represents the current binary counting value, is the output signal (Q) of all J-K flip-flop. While the output (Q) of the first J-K flip-flop is the least significant bit (LSB) of the binary value. The maximum number of counting value depends on the number of J-K flip-flops in the circuit. For example, the 4 bits counter is composed of 4 J-K flip-flops. This maximum number, which this counter can count, is 24 = 16. Hence, this counter can count from 0 to 15.

Synchronous decade counter is used to produce a count sequence from 0 to 9.in this four JK flip flops are used to count the pulses from 0 to 9 .As it is clear from the truth table .the flip flop 1 toggles on each clock pulse it.,0,1,0,1& so on .the next flip flop changes the state when Q1=1 & Q4=0.third flip flop changes its output whenQ1=Q2=1. Forth Flip flop changes its output when Q1=Q2=Q3=1or Q1&Q4=1.

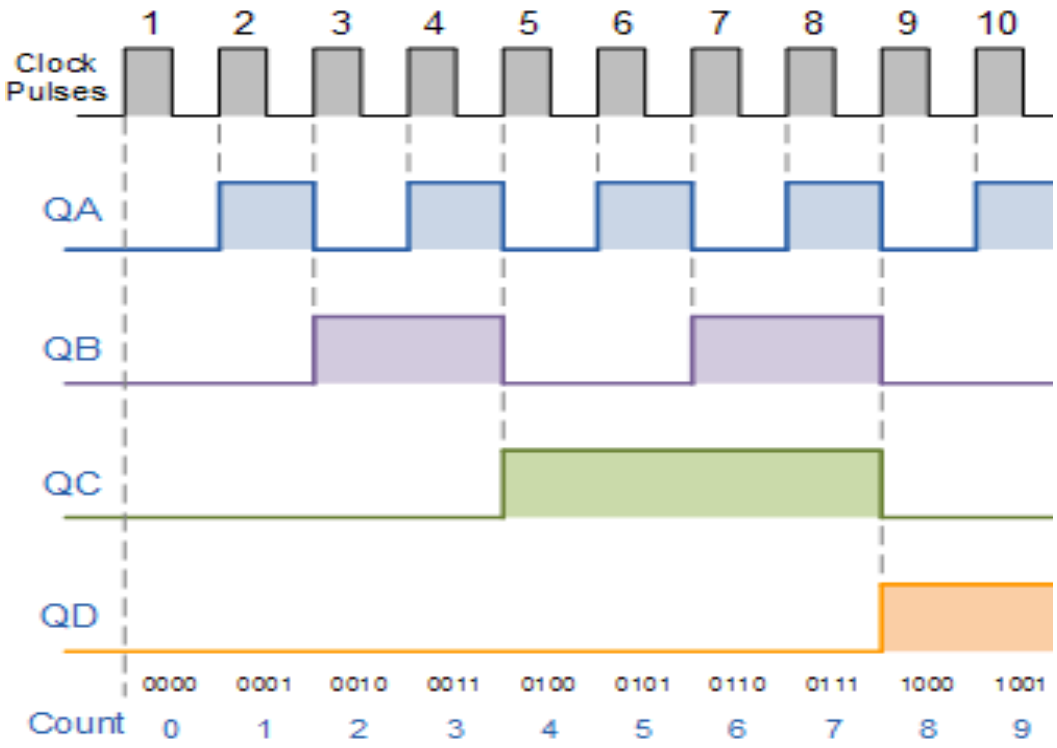
In below circuit After reaching the count of "1001", the counter recycles back to "0000". We now have a decade or **Modulo-10 counter**. the external clock signal is connected to the clock input of every individual flip-flop within the counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time. In other words there is no propagation delay.

The additional AND gates detect when the counting sequence reaches "1001", (Binary 10) and causes flip-flop FF3 to toggle on the next clock pulse. Flip-flop FF0 toggles on every clock pulse. Thus, the count is reset and starts over again at "0000" producing a synchronous decade counter.

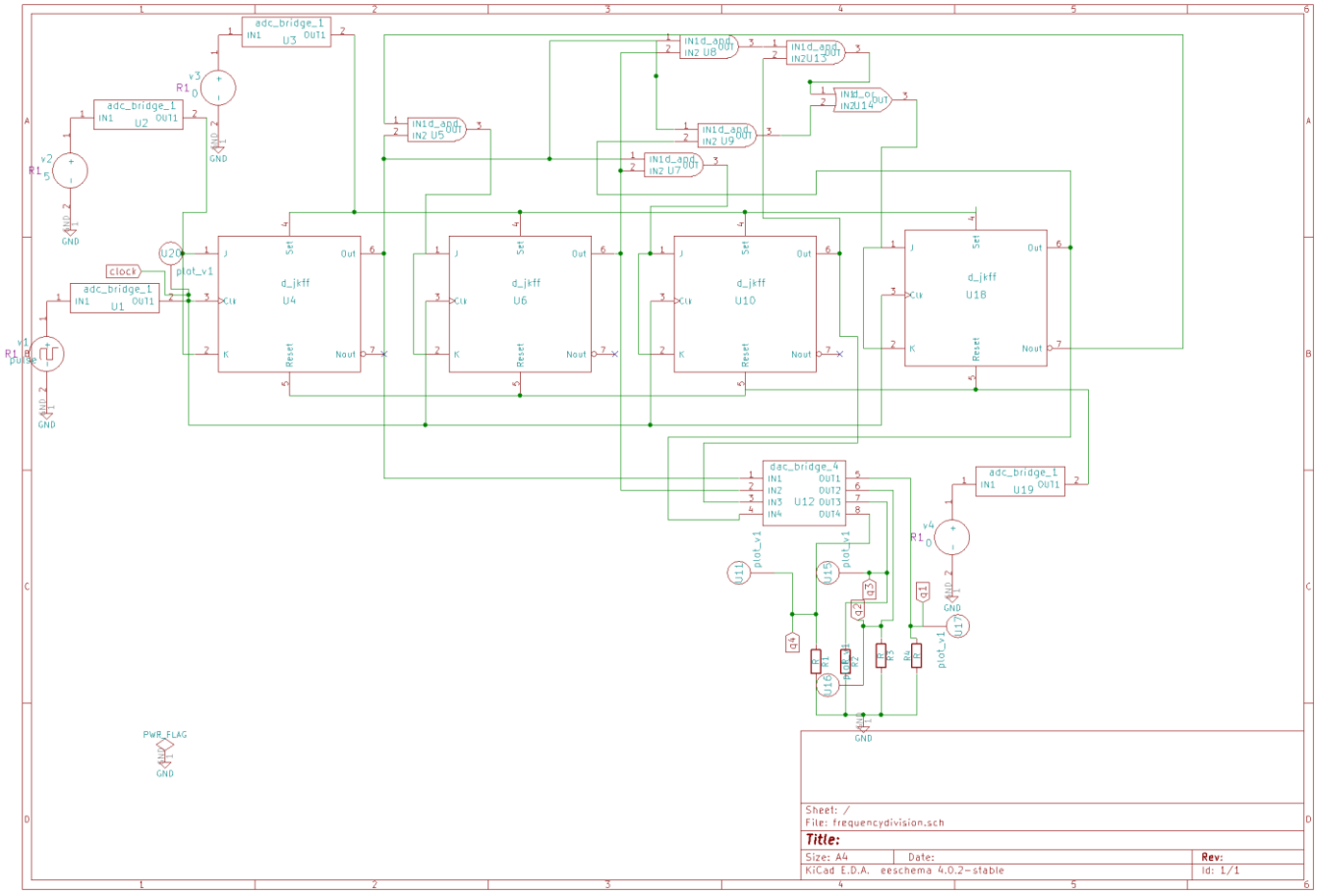
Clock pulse	Q4	Q3	Q2	Q1
0.	0	0	0	0
1.	0	0	0	1
2.	0	0	1	0
3.	0	0	1	1
4.	0	1	0	0
5.	0	1	0	1
6.	0	1	1	0
7.	0	1	1	1
8.	1	0	0	0
9.	1	0	0	1

QA=Q1,QB=Q2,QC=Q3,QD=Q4

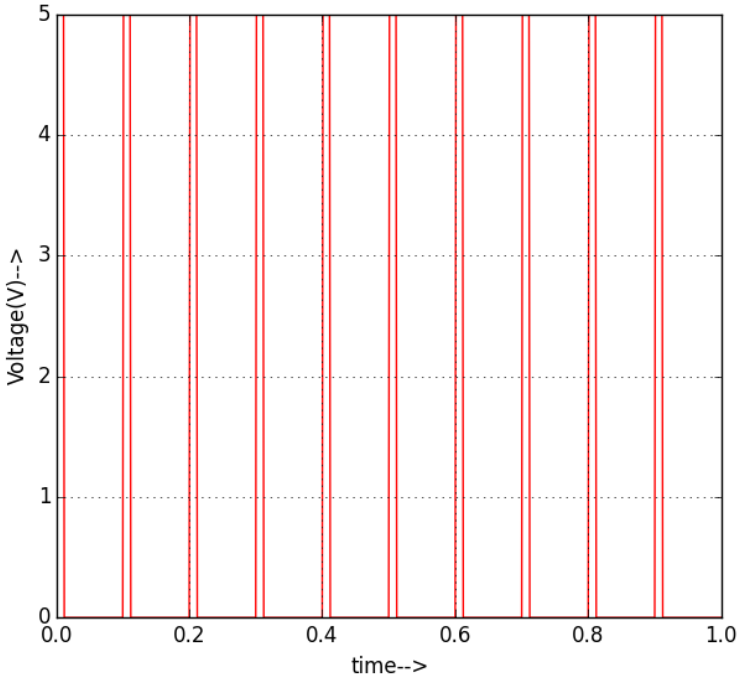
Decade counter truth table



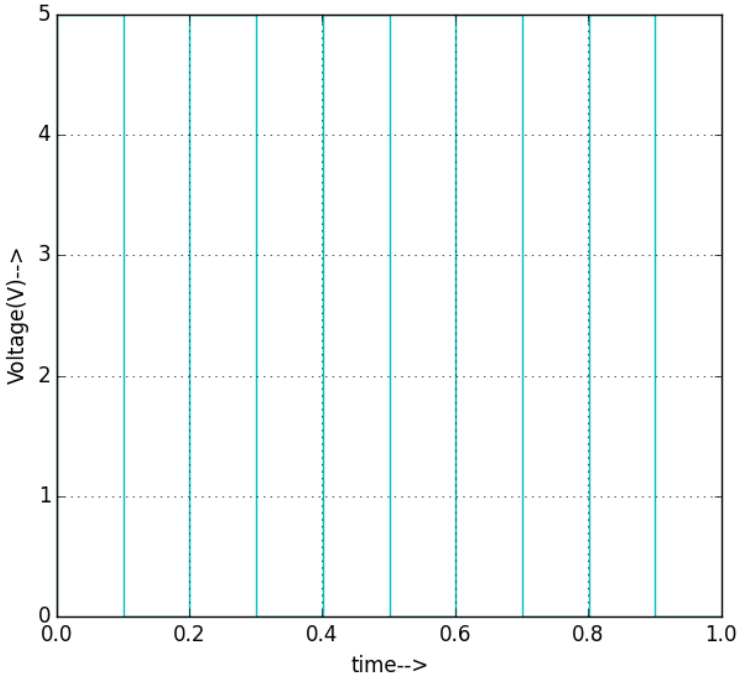
Design:



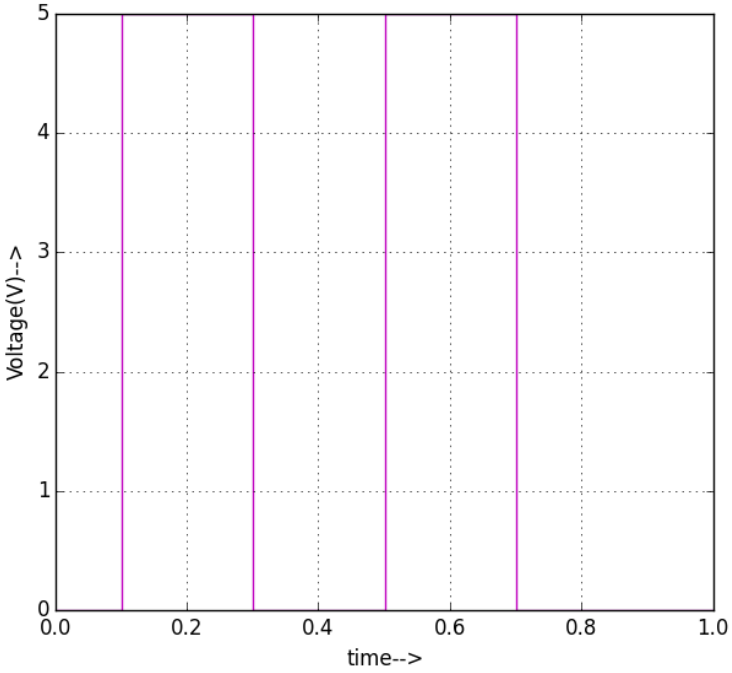
Python plots



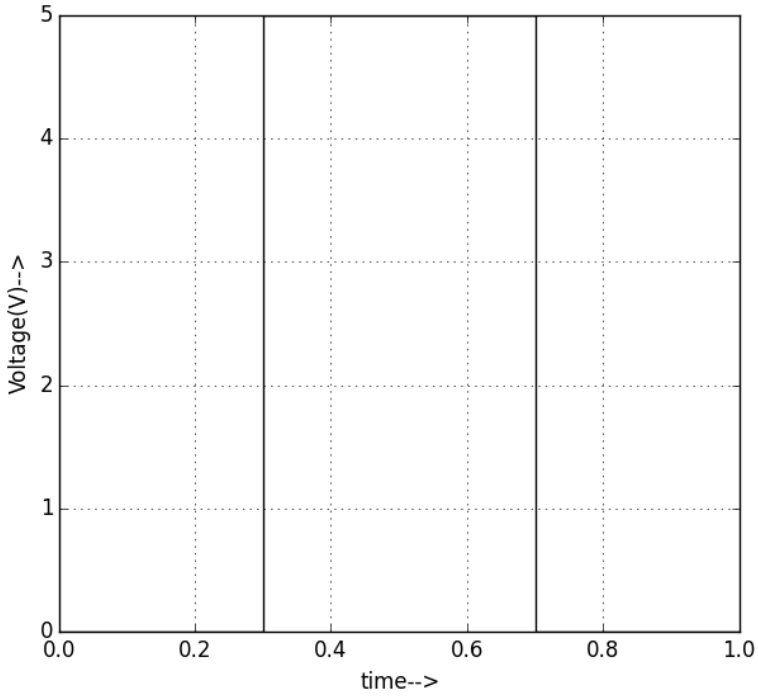
Input clock Waveform



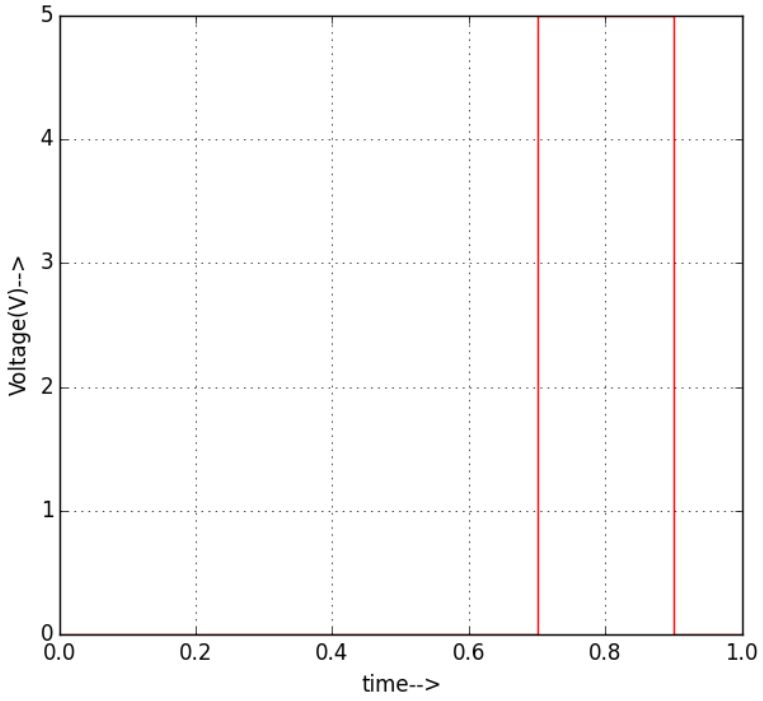
Waveform of Output q1



Waveform of Output q2

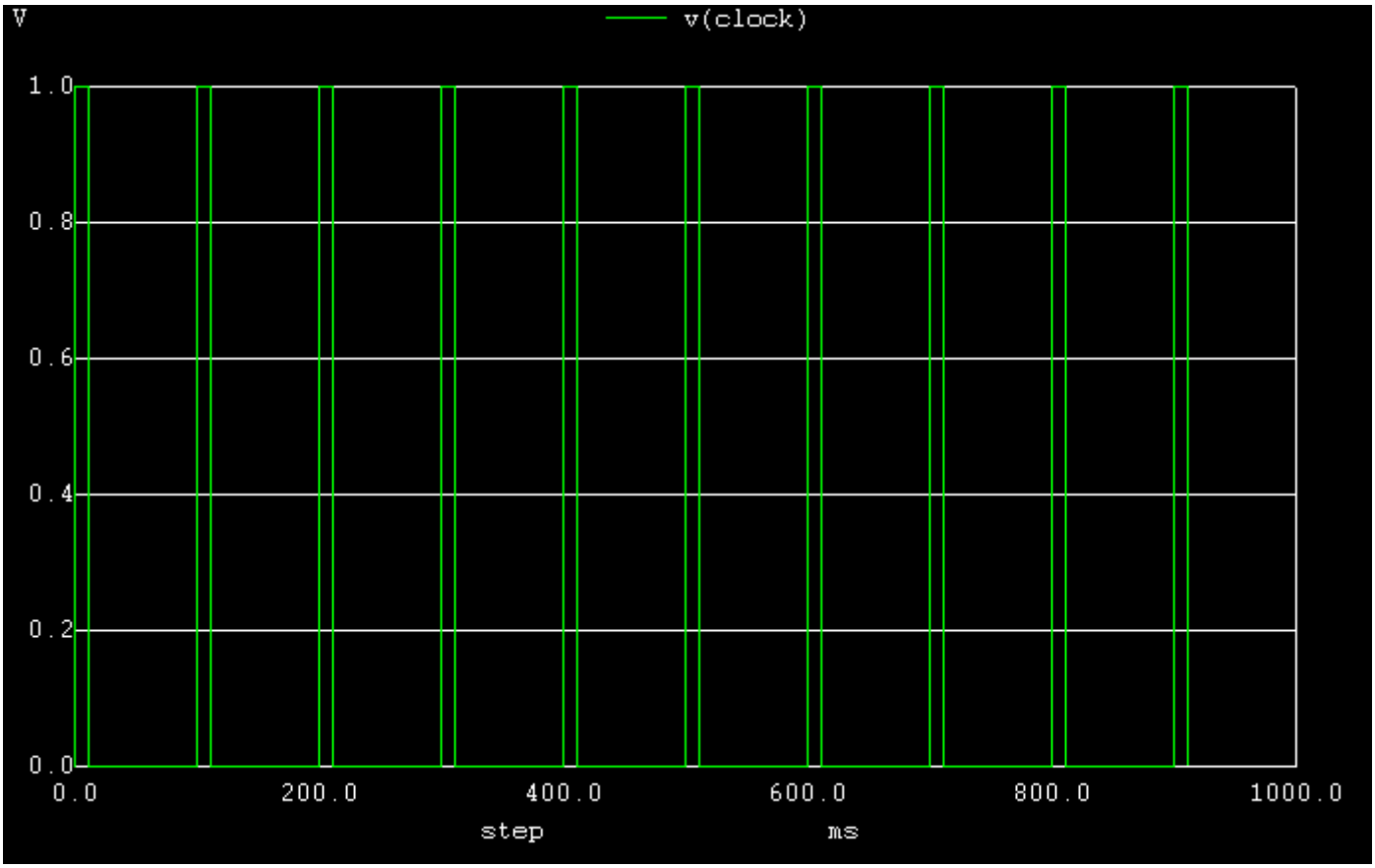


Waveform of Output q3

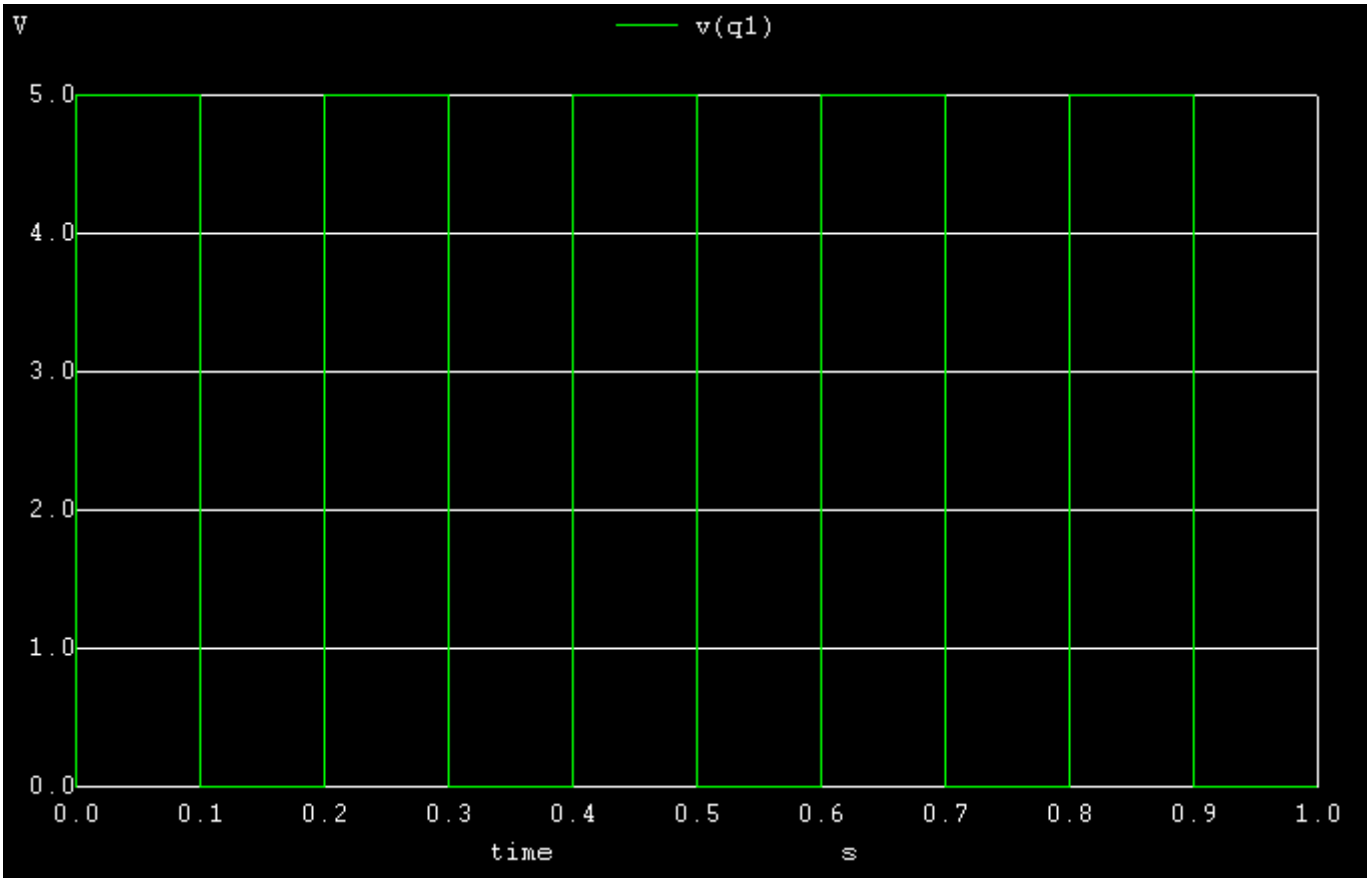


Waveform of Output q4

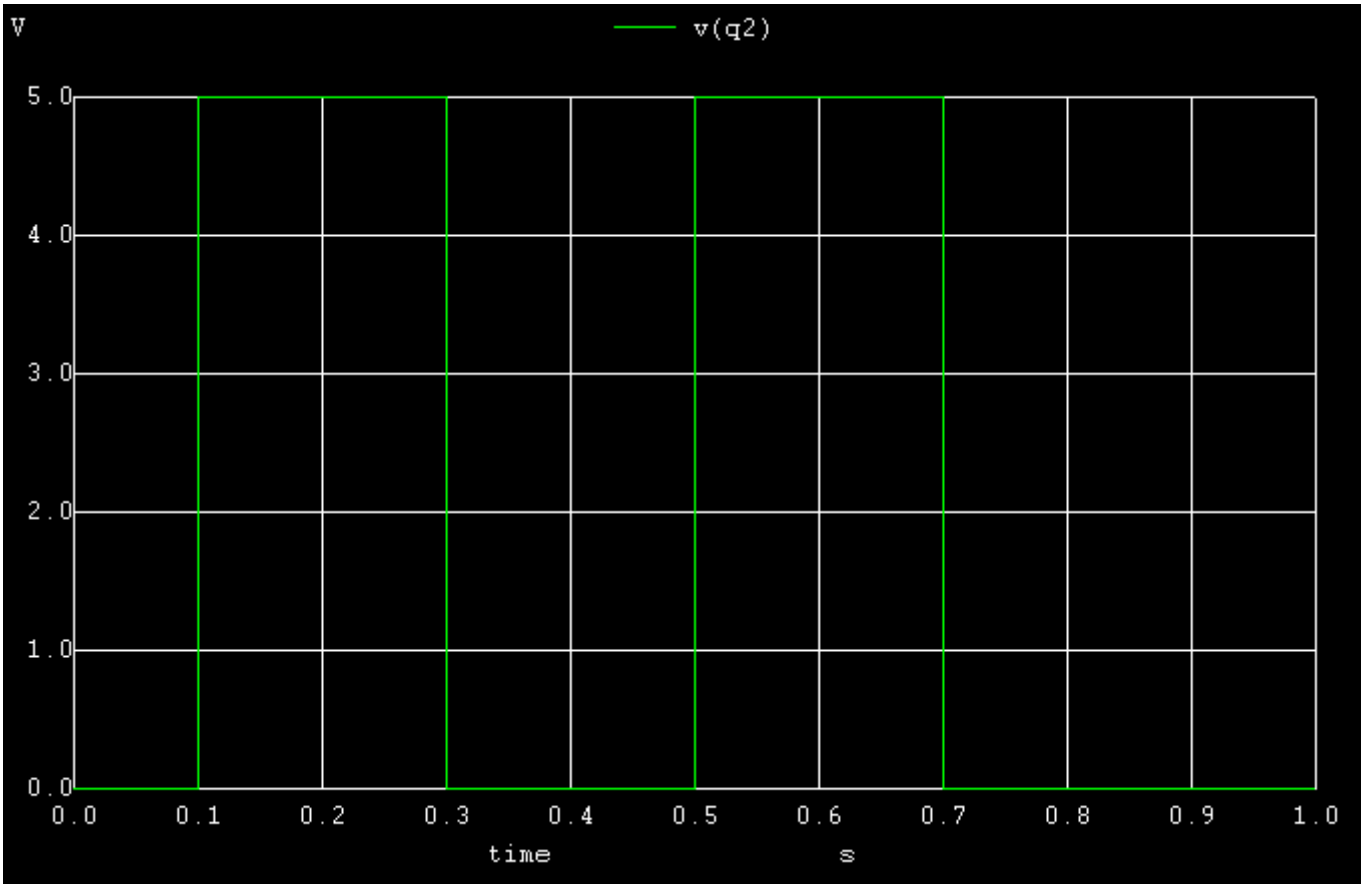
Ngspice plots:



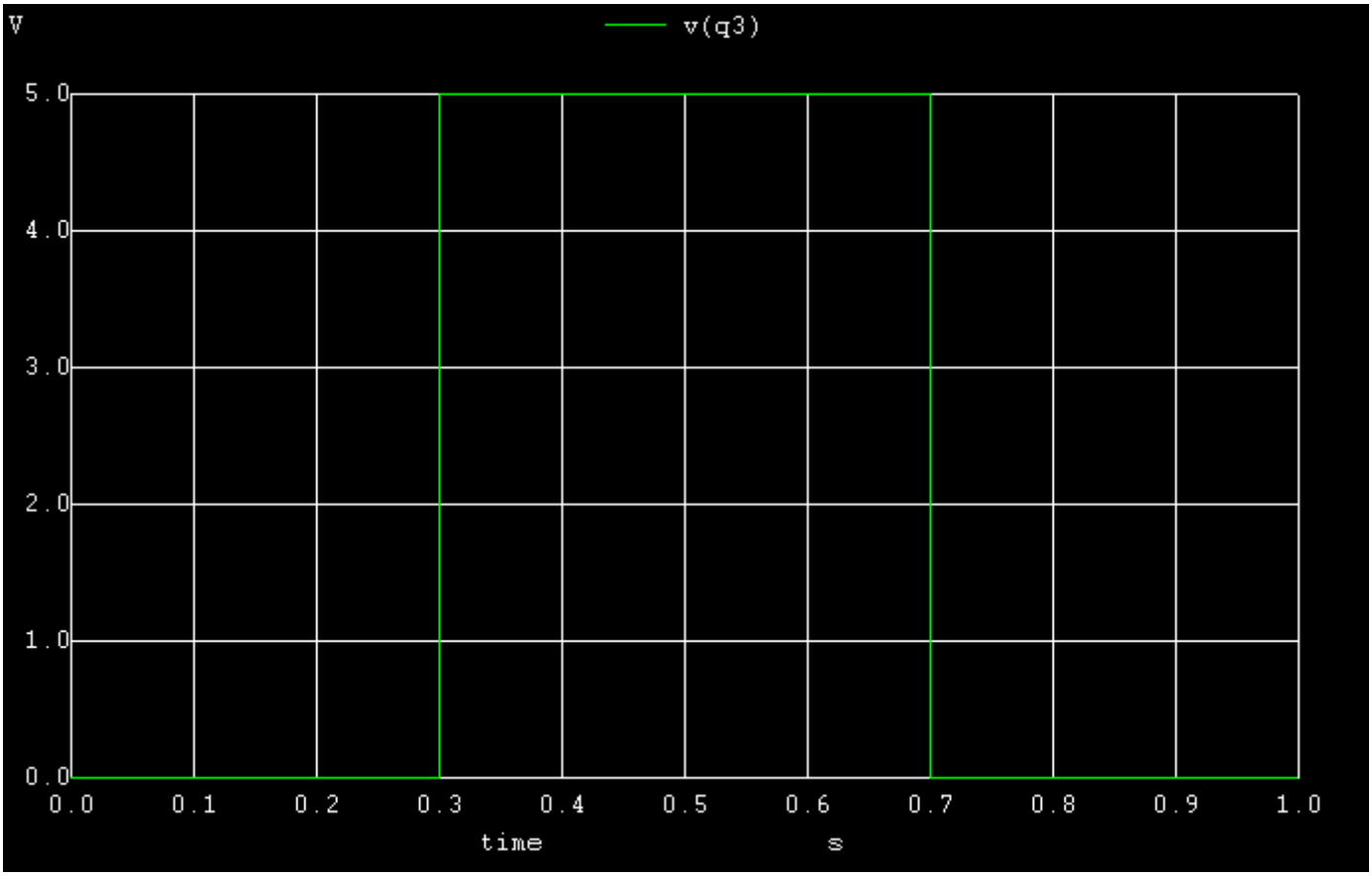
Input Clock Waveform



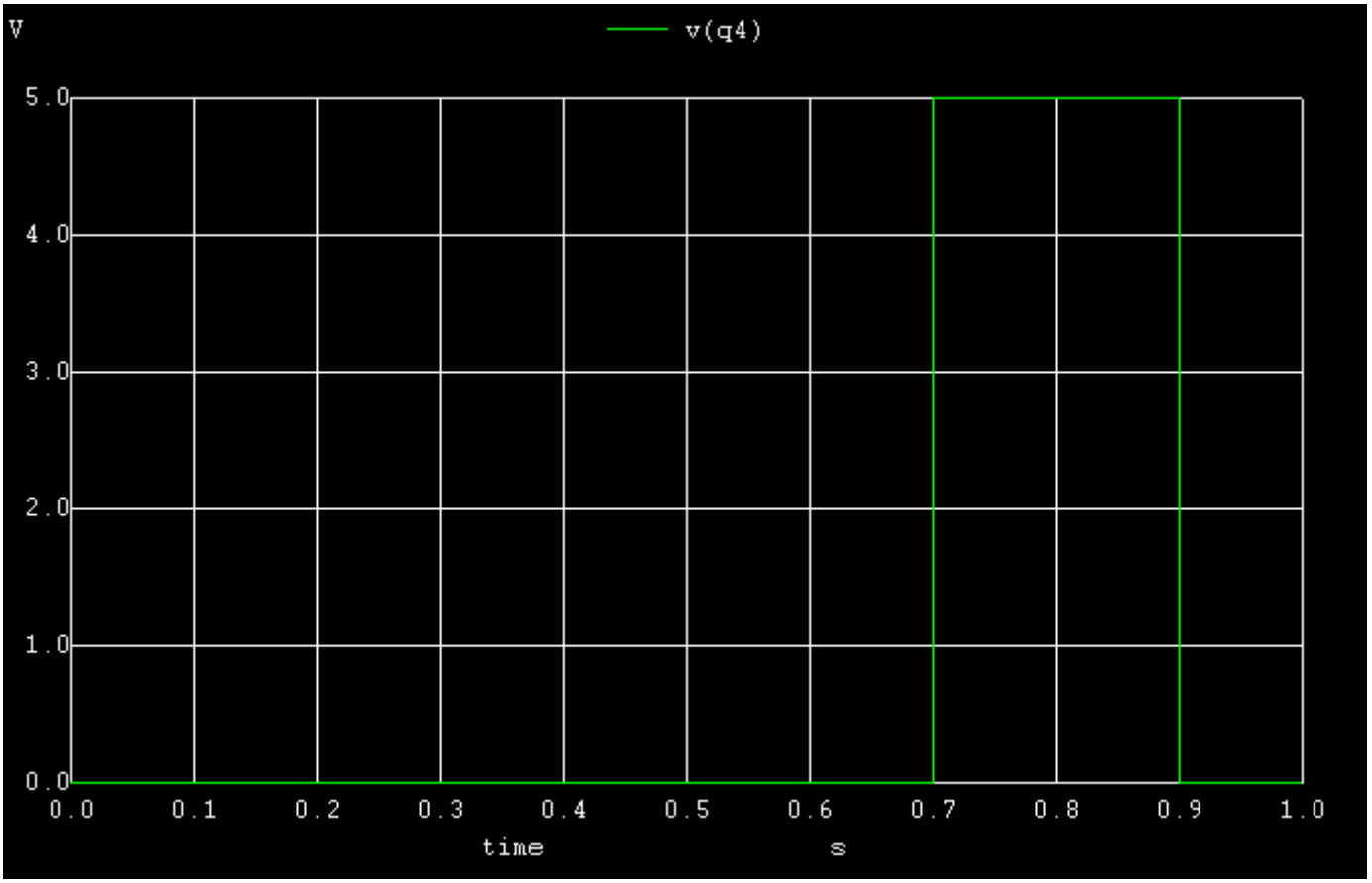
Ngspice Output plot of q1



Ngspice Output plot of q2



Ngspice Output plot of q3



Ngspice Output plot of q4

Reference:

https://www.ee.usyd.edu.au/tutorials/digital_tutorial/part2/counter06.html

https://www.electronics-tutorials.ws/counter/count_3.html