

DESIGN AND ANALYSIS OF RING OSCILLATOR CMOS CIRCUIT AT 65 NM TECHNOLOGY

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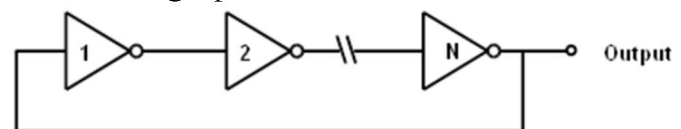
Title of the circuit: Design and Analysis of Ring Oscillator CMOS circuit at 65 nm Technology

• ABSTRACT:

This paper presents a CMOS ring oscillator designed for low power applications using 65 nm CMOS technology. A ring oscillator, comprising an odd number of NOT gates, generates oscillations by alternating between two voltage levels. The proposed design is compact and operates at high speed, making it ideal for integration in random number generators and other low-power systems. Simulated using the eSim tool, the oscillator operates with an average power consumption of 25.48 nanowatts at a 1V supply voltage, significantly reducing power compared to conventional designs. This advancement demonstrates the feasibility of integrating low-power oscillators in high-performance, energy-efficient VLSI applications.

• INTRODUCTION

A ring oscillator is an odd number (N) of inverting stages connected in series with the output fed back to the input as shown in the below figure. A ring oscillator can be made with a mixture of inverting and non-inverting stages, provided the total number of inverting stages is odd. The ring oscillator and related circuits are fundamental building blocks used as clock oscillators in computers and carrier frequency generator phase locked loops in wireless communications. It is also a fundamental circuit for evaluating the intrinsic speed of a CMOS logic process.



• DESIGN AND WORKING OF A CMOS RING OSCILLATOR

The CMOS ring oscillator is a versatile circuit widely used in digital and analog applications because of its simple structure and compatibility with low-power CMOS technology. This oscillator consists of a series of inverters—an odd number of NOT gates—arranged in a closed loop, where the output of the last inverter is fed back to the input of the first. Each inverter flips the input signal, causing oscillations to form as the circuit stabilizes between two voltage levels representing logical "1" and "0."

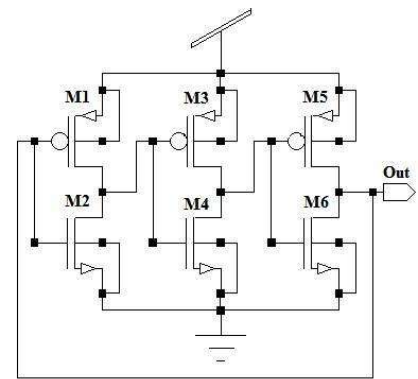
• DESIGN OF THE CMOS RING OSCILLATOR

In the CMOS ring oscillator, an odd number of inverter stages is essential for oscillation. This configuration is chosen because it meets the Barkhausen criterion for oscillation: the total phase shift around the loop must be 360 degrees, and the loop gain must equal one. Each inverter introduces a 180-degree phase shift, so an odd number of inverters allows the signal to experience a total 180-degree shift with feedback, creating continuous oscillations. For this design, 65 nm CMOS technology is used. At this technology node, the circuit's dimensions are minimized, allowing the oscillator to consume less power and occupy less area. Operating at a supply voltage of 1V, this design achieves an average power consumption of just 25.48 nanowatts, making it efficient for applications where power conservation is essential.

• WORKING PRINCIPLE OF THE CMOS RING OSCILLATOR

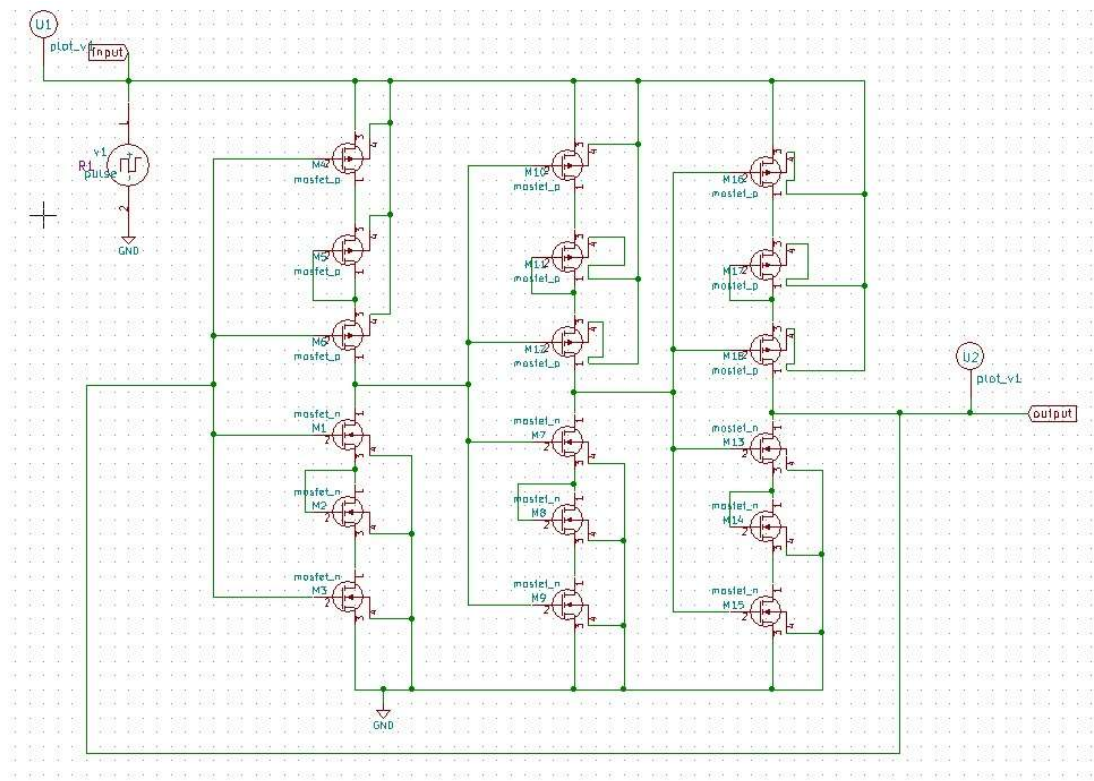
The ring oscillator operates as a series of signal inversions. When a voltage is applied to the first inverter, the output oscillates as each inverter successively flips the signal. This oscillation continues through each inverter stage, returning to the input of the first inverter, where it repeats the process. This cycle produces an output that alternates between high and low states, generating a periodic waveform.

Due to the cascading inverters, the circuit creates a time delay through each stage, which determines the oscillator's frequency. The total delay through all inverter stages sets the period of oscillation. As each inverter introduces a delay based on its design and the operating conditions, the total delay across the odd-numbered chain of inverters dictates the frequency. This delay is directly influenced by the supply voltage, technology node, and the width-to-length ratio of the transistors.

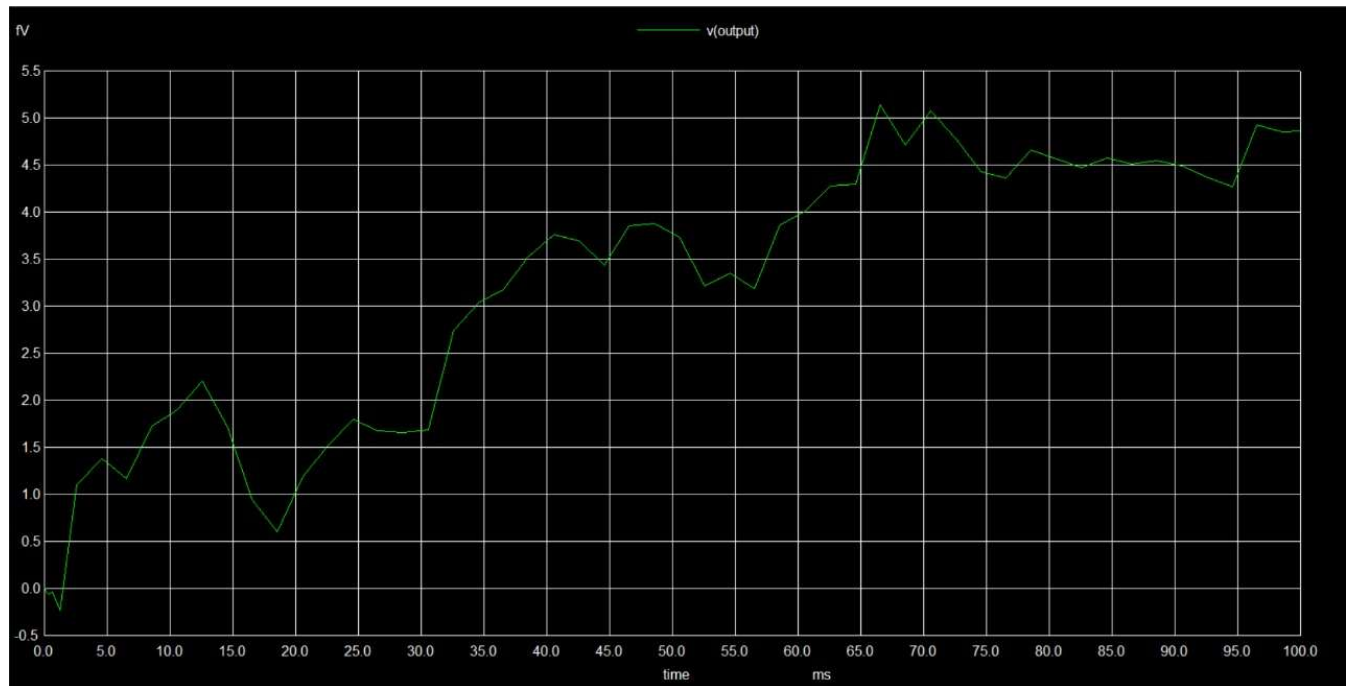


• **SCHEMATIC DIAGRAM:**

The circuit schematic of CMOS Ring Oscillator using 180nm technology in eSim is as shown below:



• **SIMULATION RESULTS:**



Output waveform at 1v supply voltage in 65 nm technology

- **CONCLUSION**

This project successfully demonstrates the design and analysis of a CMOS ring oscillator using 65 nm technology, optimized for low power applications. By leveraging the simplicity of CMOS inverters in an odd-numbered ring configuration, the oscillator achieves reliable oscillations with minimal power dissipation

- **REFERENCES**

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[Activity: CMOS Inverter Ring Oscillator \[Analog Devices Wiki\]](#)
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