Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Design and Simulation of a CMOS Bandgap Reference Voltage Circuit with Start-up Circuit using eSim

Theory/Description : A bandgap reference (BGR) circuit is used to generate a stable reference voltage that remains nearly constant despite variations in temperature, supply voltage, and process parameters. This type of circuit is widely used in analog and mixed-signal systems such as ADCs, DACs, voltage regulators, and sensor interfaces.

The working principle of the bandgap reference is based on combining two voltages with opposite temperature characteristics. One is a CTAT (Complementary To Absolute Temperature) voltage obtained from a diode-connected device, which decreases with temperature. The other is a PTAT (Proportional To Absolute Temperature) voltage generated using the difference between diode voltages, which increases with temperature.

By properly scaling and adding these two components, the temperature effects cancel each other, resulting in a nearly constant output voltage close to the silicon bandgap (~1.2V). A current mirror is used to maintain proportional currents in different branches of the circuit.

Since the circuit is self-biased, a start-up circuit is included to ensure that the circuit does not remain in the zero-current state during power-on and reliably reaches its normal operating condition.

Reason to reproduce with eSim : This circuit is well-suited for implementation in eSim because it involves transistor-level analog design, which can be effectively simulated using ngspice and standard CMOS models available in eSim.

eSim provides an open-source platform to replicate such circuits without requiring expensive tools like Cadence. It also allows easy analysis of temperature variation, supply sensitivity, and transient behavior.

Reproducing this circuit in eSim helps in understanding practical analog design concepts such as current mirrors, temperature compensation, and biasing techniques. It also gives an

opportunity to validate results from the research paper and explore possible improvements like power optimization or better temperature stability.

Expected Outcome/outputs : **When the circuit is simulated, it is expected to generate a stable reference voltage around 1.2V. The output voltage should remain nearly constant over a wide temperature range and under supply voltage variations.**

The PTAT voltage should show a positive slope with temperature, while the CTAT voltage should show a negative slope. The combined output should remain flat, indicating proper temperature compensation.

The start-up circuit should ensure that the output voltage rises from 0V to its steady value during power-on and does not remain stuck in the zero-current condition.

Circuit Diagram(s) :

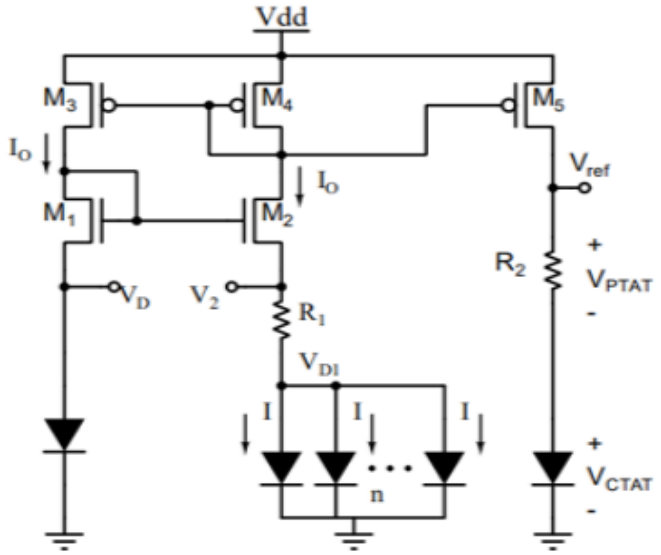


Fig.4. Diagram of the BGR circuit where both PTAT and CTAT circuits are summed up together

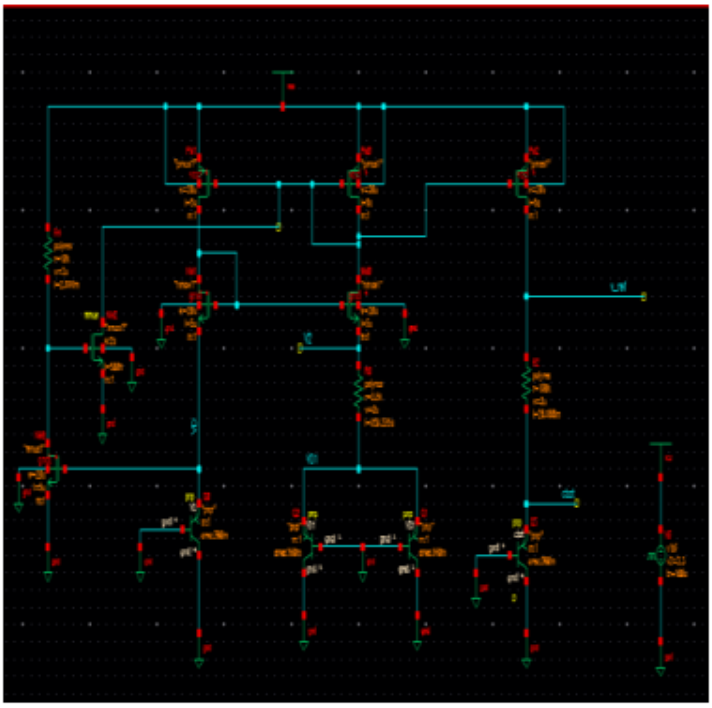
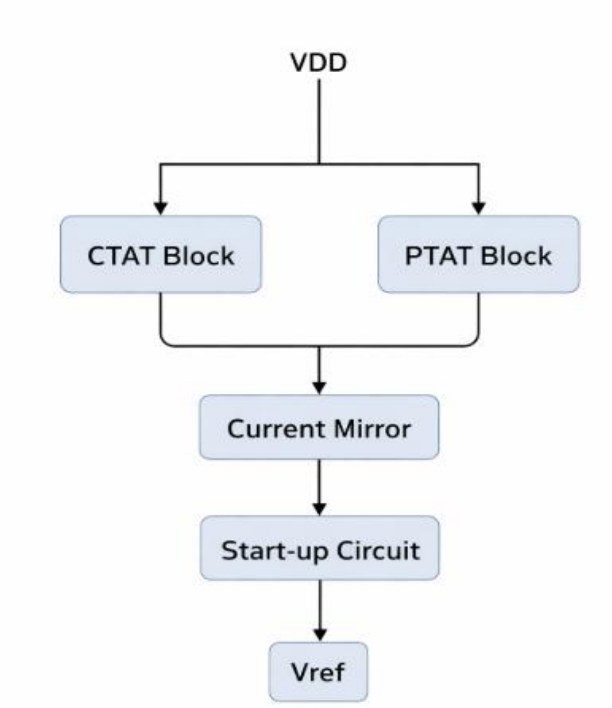


Fig.5. Schematic of Design of Startup circuit

Block Diagram (s) :



Block Diagram of Bandgap Reference Circuit

Expected Results (Input, Output waveforms and/or Multimeter readings) :

1. Transient Response:

- **Output should rise from 0V → ~1.2V**
- **Shows proper startup operation**

2. Temperature Sweep:

- **CTAT: decreasing line**
- **PTAT: increasing line**
- **Vref: nearly constant**

3. Output Voltage:

- **Around 1.1V – 1.25V (depending on model)**

4. Supply Variation:

- **Vref should remain stable even if Vdd changes**

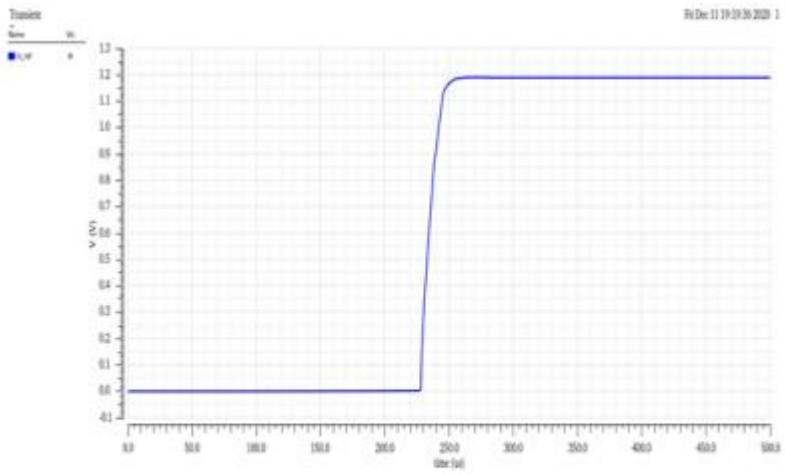


Fig.6. When the circuit is off, the BGR circuit stays at 0 V. When the startup circuit activates, the circuit turns on and rises up to 1.2 V.

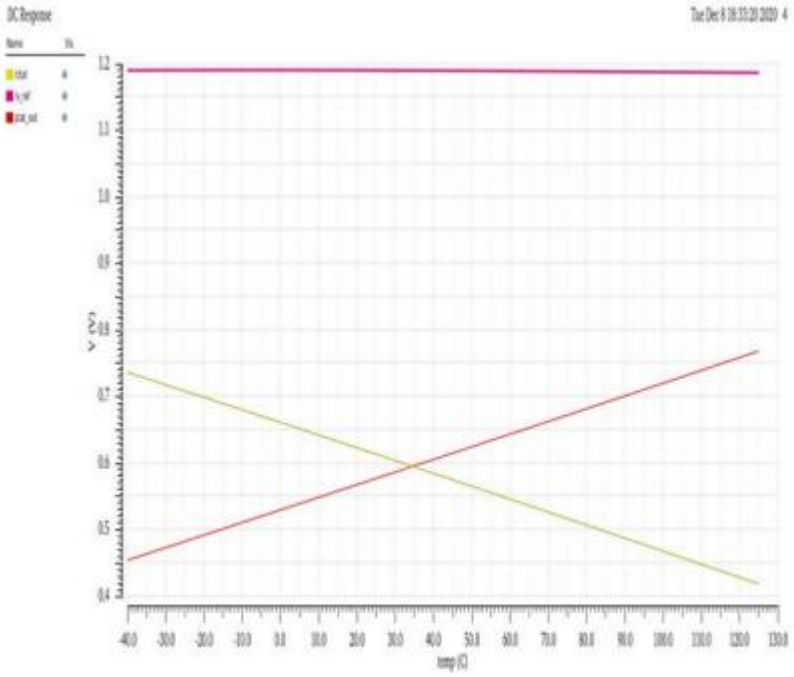


Fig. 7. Output graph of the Bandgap reference voltage

Research Paper/Journal/etc. :

Title : Design and Simulation of CMOS based Bandgap Reference Voltage with Start-up Circuit using 180 nm, 90 nm and 45 nm Process Technology

Author : Akshaya Anand, Sreenidhi P.R

Page No. : 1078–1083

Link : https://ieeexplore.ieee.org/document/9785154

Source/Reference(s) :

1 Behzad Razavi, *Design of Analog CMOS Integrated Circuits*

2 IEEE papers on Bandgap Reference

3 FOSSEE eSim documentation

4 Basic MOSFET and current mirror theory notes
