Design and Analysis of Ring Oscillator CMOS circuit at 65 nm Technology

Name of the participant: Hamim Reja

University: Aliah University

Title of the circuit: Design and Analysis of Ring Oscillator CMOS circuit at 65 nm Technology

- **Problem Statement:**

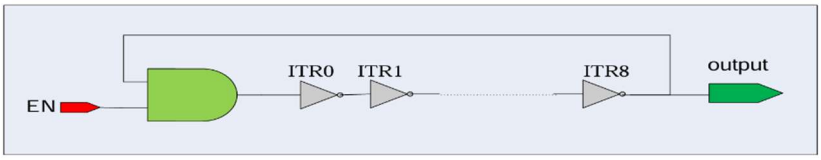
  The objective is to design a CMOS ring oscillator at 65 nm technology that achieves low power consumption while maintaining high-speed performance. Traditional oscillator designs typically exhibit high power dissipation, which restricts their efficiency in applications requiring compact, low-power solutions. This project addresses the need for a more energy-efficient and space-saving oscillator that can operate effectively in various low-power VLSI applications, such as random number generators and high-speed data processing modules.

- **Theory:**

  Here I have to simulate a Ring Oscillator using CMOS circuit at 65nm technology, which is already done by Nauneet Kumar Mehta, Bhagwat Kakde, Ramji Gupta, Bharti Chourasia in Cadence Virtuoso tool. In this project I have try to simulate, the ring oscillator operates based on the principle of an odd-numbered sequence of inverters connected in series, where the output of the last inverter is feedback into the input of the first, enabling continuous oscillation. This configuration leverages Barkhausen's criteria for oscillation, achieving a 360-degree phase shift with unity gain. Unlike LC-tank oscillators, ring oscillators are compact and suitable for integration in low-power, high-speed environments. The circuit's performance is defined by the delay of each inverter stage, and power dissipation is minimized through the efficient CMOS design, making it well-suited for applications like phase-locked loops and high-speed data modules.

- **Circuit Diagram:**

  A ring oscillator is a device composed of odd number of NOT gates, the output of these NOT gates oscillates between two different voltage levels, representing logic 1 and logic 0. Theses inverters are cascaded in series and the output of the last inverter is feedback into the first. CMOS ring oscillator uses only odd number of inverter stages because even number of stages gives same output so oscillation cannot be produced. Below Fig. shows the schematic diagram of n-stage ring oscillator using n number of inverters, AND gate with enable input.



- **Source/Reference(s):**

  - **Title of the paper:** Design and Analysis of Ring Oscillator CMOS circuit at 65 nm Technology
  - **Name of the publication:** *IJPUBLICATION | IJRAR | www.ijrar.org | E-ISSN 2348-1269, P- ISSN 2349-5138*
  - **Authors:** Nauneet Kumar Mehta, Bhagwat Kakde, Ramji Gupta, Bharti Chourasia.
  - **Pages, Published in:** 338-341 | Volume 6 | Issue 2 | June 2019.
  - **Link:** http://ijrar.org/viewfull.php?&p_id=IJRAR