Circuit Simulation Project

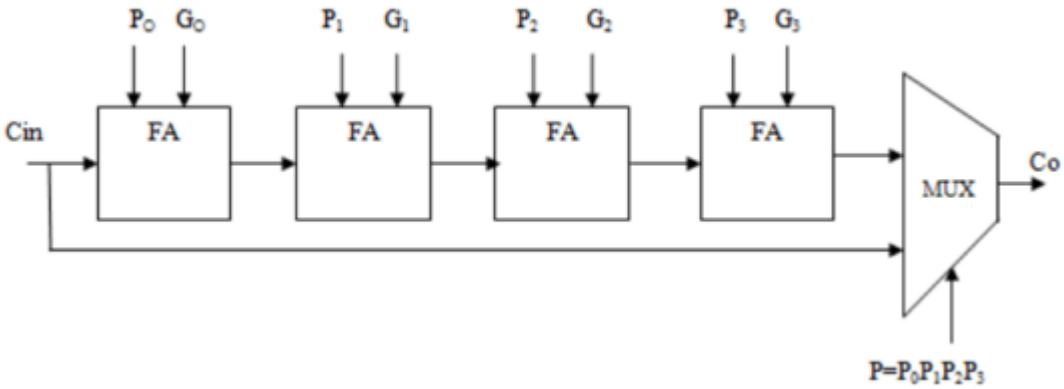
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Jovin P John

Title of the circuit : 4 Bit Carry Bypass Adder

Theory/Description : A 4-bit Carry Bypass Adder is a circuit that adds two 4-bit binary numbers using full adders to produce the sum outputs and the final carry. Unlike a simple ripple-carry adder, it also checks whether the carry can skip all four stages through a shortcut path. This decision is controlled by the block propagate signal p, defined as p = p0·p1·p2·p3, where each pi = ai XOR bi. If p = 1, a multiplexer forwards the input carry directly to the output carry for faster operation, while if p = 0, the carry ripples through the adders in the normal way.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

a3a2a1a0 | b3b2b1b0 | c0 | s3s2s1s0 | c4 | p

0000 | 0000 | 0 | 0000 | 0 | 0

0000	0000	1	0001	0	0
0001	0001	0	0010	0	0
0001	0001	1	0011	0	0
0010	0010	0	0100	0	0
0010	0010	1	0101	0	0
0011	0011	0	0110	0	0
0011	0011	1	0111	0	0
0100	0100	0	1000	0	0
0100	0100	1	1001	0	0
0101	0101	0	1010	0	0
0101	0101	1	1011	0	0
0110	0110	0	1100	0	0
0110	0110	1	1101	0	0
0111	0111	0	1110	0	0
0111	0111	1	1111	0	0
1000	1000	0	0000	1	0
1000	1000	1	0001	1	0
1001	1001	0	0010	1	0
1001	1001	1	0011	1	0
1010	1010	0	0100	1	0
1010	1010	1	0101	1	0
1011	1011	0	0110	1	0
1011	1011	1	0111	1	0
1100	1100	0	1000	1	0
1100	1100	1	1001	1	0
1101	1101	0	1010	1	0
1101	1101	1	1011	1	0
1110	1110	0	1100	1	0
1110	1110	1	1101	1	0

1111 | 1111 | 0 | 1110 | 1 | 0

1111 | 1111 | 1 | 1111 | 1 | 0

Source/Reference(s) : Sunitha, G. S., & Rakesh, H. M. (2017). Design and implementation of adder architectures and analysis of performance metrics. *International Journal of Electronics and Communication Engineering and Technology (IJECET)*