Circuit Simulation Project

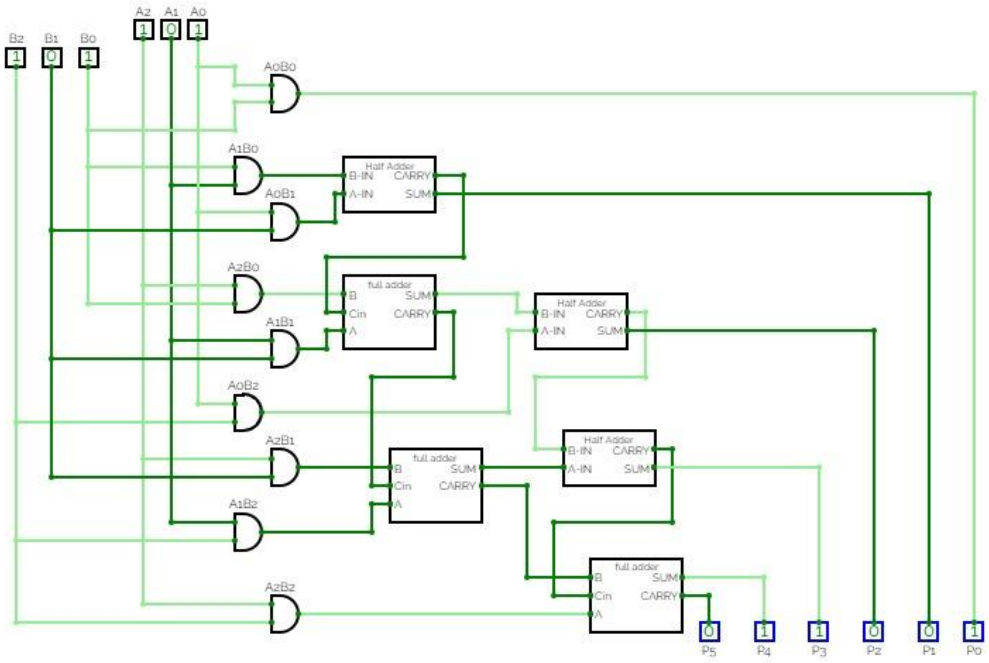
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Jovin P John

Title of the circuit : 3x3 Array Multiplier

Theory/Description : A **3×3 array multiplier** is a digital circuit that multiplies two 3-bit binary numbers to produce a 6-bit binary product. It works by generating nine partial products using AND gates—each bit of one input is ANDed with each bit of the other—and then summing these partial products using half-adders and full-adders arranged in an array. The result is a straightforward, combinational way to perform binary multiplication, where the output directly represents the product of the two 3-bit inputs.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

A (dec)	A (bin)	B (dec)	B (bin)	Product (dec)	Product (bin, p5...p0)
0	000	0	000	0	000000
1	001	1	001	1	000001
2	010	2	010	4	000100
3	011	3	011	9	001001
4	100	4	100	16	010000
5	101	5	101	25	011001
6	110	6	110	36	100100
7	111	7	111	49	110001

Source/Reference(s) : D. T. Raju and M. D. S. Manasa, “Design and Implementation of 3*3 Array Multiplier using DPTL Logic,” *International Journal of Engineering Research & Technology (IJERT)*