# 3-bit Synchronous up counter with buffered reset

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***Abstract*— Counters are digital circuits widely used in various applications like counting, frequency divisions, memory increment in the registers, etc. In this abstract, the design of a 3-bit up counter is described where the reset is buffered using a CMOS inverter buffer for better performance.**

## I. REFERENCE CIRCUIT DETAILS

The circuit is to be designed on SkyWater 130 pdk on esim software. The asynchronous reset for the counter is specially buffered to avoid the issue of weak reset which could lead to the counter not getting reset when required by the user. The buffer circuit is designed using connecting back-to-back 2 CMOS digital inverters [1][2] to keep the buffer area efficient yet good in performance.

## II. REFERENCE CIRCUIT DESIGN

The proposed schematic of the design is shown in Fig 1.

| S.no | Design Component | Description |
|---|---|---|
| 1 | Inverter | To be designed using ng-spice |
| 2 | A/D & D/A | Converter bridges to be used |
| 3 | Counter | On Verilog and converted to spice netlist for mixed-signal abstraction |
| 4 | CLK, RST | Standard pulse sources in the spice library |

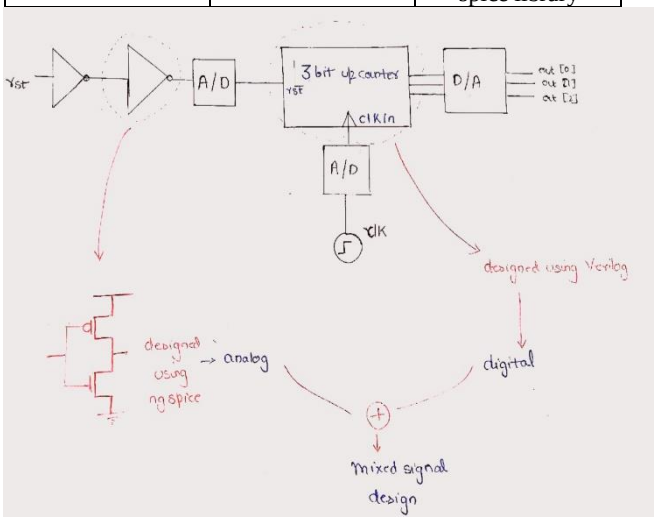


Fig 1: Proposed Circuit Schematic and Abstraction [3]

## III. REFERENCE WAVEFORM

The operation of the counter along with the enabling of asynchronous reset is shown in Fig 2.

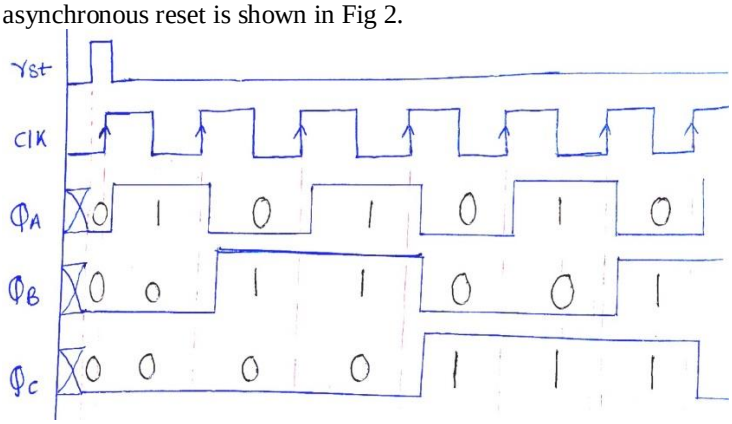


Fig 2: Proposed Circuit Waveform

## REFERENCES

[1] Maekawa, Tomoaki & Amakawa, Shuhei & Ishihara, Noboru & Masu, Kazuya. (2009). Design of CMOS inverter-based output buffers adapting the Cherry-Hooper broadbanding technique. 511 - 514. 10.1109/ECCTD.2009.5275025.

[2] Mariyamol, p.p & Aswathy, N.. (2016). CMOS Buffer Design Approach for Low Power and Lower Delay SRAM Design. Procedia Technology. 25. 481-488. 10.1016/j.protcy.2016.08.135.

[3] Thomas L. Floyd "Digital Fundamentals", 11th ed global edition, pp. 507-527