Design of JK flip flop using mixed signals

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Abstract: **This electronic document is about the designing of a JK flip flop using mixed signals. Flip flops are the fundamental blocks of memory devices. There are four types of flip flops, here we are about to see the JK flip flop.**

1. Introduction

The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. The JK flip flop functions similarly to the SR flip flop. Instead of "S" and "R," the JK flip flop bears the letters "J" and "K." In contrast to SR flip flops, which produce invalid states as outputs when both inputs are set to 1, JK flip flops do not produce invalid states even when both "J" and "K" flip flops are set to 1. This is the only difference between JK flip flops and SR flip flops.

2. Working

The JK flip-flop is basically an SR flip flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time under normal switching thereby eliminating the invalid condition seen previously in the SR flip flop circuit. However, if both the J and K inputs are HIGH at logic “1” (J = K = 1), when the clock input goes HIGH, the circuit will “toggle” as its outputs switch and change state complementing each other. This results in the JK flip-flop acting more like a T-type toggle flip-flop when both terminals are “HIGH”.

3. Implementation

Here, we use an Analog to Digital converter to introduce the binary input to the JK flip flop at the circuit's beginning, and we use a Digital to Analog converter to return the output of the JK flip flop to analogue form. By utilising mixed signals, we can create a JK flip flop in this manner.

4. Block diagram