Mixed Signal SoC VGA Clock

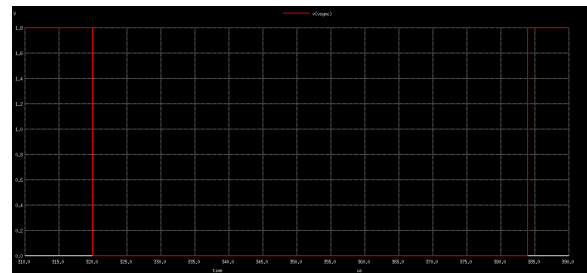**Vishal Sivakumar, Mahindra University**
October 30, 2022

Abstract—Goal is to design a mixed signal SoC which can display time through 640x480@60Hz VGA interface. It needs an input of 25MHz, fed through a current limiting resistor. This forms its analog part. Digital parts implement a FSM for counting time in 24 Hr format and generate display signals required for VGA interface. Pins are designed on the top module to adjust hour, minute and second.
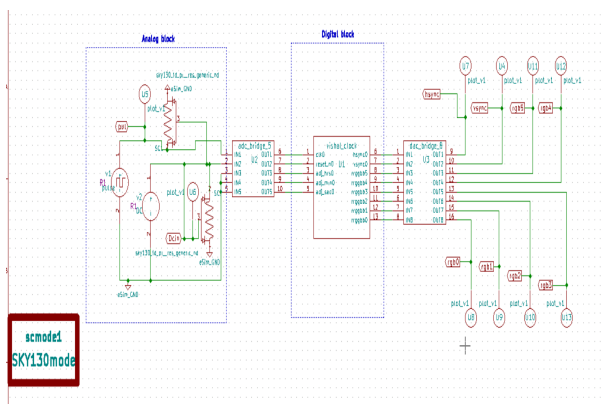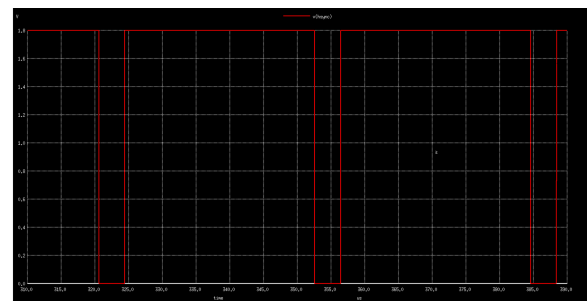
Implemented Circuit Details- Analog part simply consists of few current limiting resistors to save the SoC in times of sudden short circuit. In the digital part, there is a display signal generation block to generate hsync and vsync signals for VGA, with the help of display timing information and a drawing logic block which implements the clock as FSM. The latter is also responsible for rendering time onto screen through red, blue and green channels by reading data from ROM implemented for fonts and various .hex files included.

Implemented Waveforms-

Vsync signal

Hsync signal

References for design and ip cores-

- https://github.com/mattvenn/vga-clock.git
- https://projectf.io/posts/hardware-sprites/
- https://github.com/projf/projf-explore