HALF ADDER USING CMOS

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ABSTRACT:

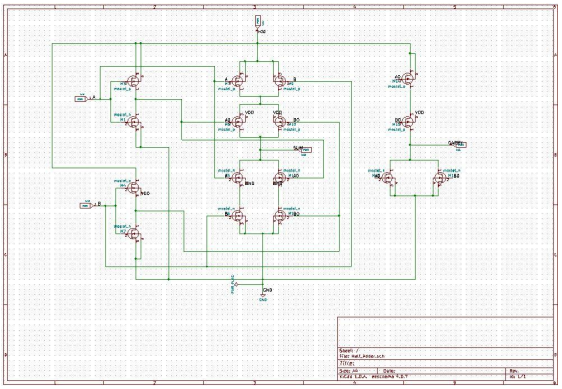
Half Adder is the digital logic circuit which adds two single bit binary numbers and gives two outputs. The inputs are A, B and outputs are SUM, CARRY. Half Adder will do binary addition of A and B and will give the sum of two inputs at SUM and carry bit at CARRY. We can also see the output using Circuit Waveform. Generally, in various types of processors, adders are used to perform arithmetic and logical operations. Half Adder is implemented using CMOS.

REFERENCE CIRCUIT DETAILS:

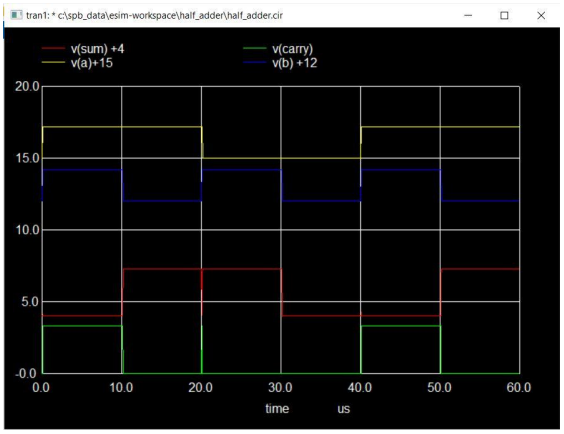
Complementary Metal Oxide Semiconductor (CMOS) logic deploys symmetric number of both types of MOSFETs, i.e., PMOS and NMOS. Half Adder using CMOS is modelled using 12 Transistors. Half Adder is a digital circuit which will add two binary inputs and will give two outputs, SUM and CARRY. The two inputs are A, B and outputs are SUM and CARRY. As we have 2 inputs we will have 4 input combinations.

The addition of 2 inputs will occur at SUM output and carry bit will occur at CARRY output. For SUM circuit, The PMOS circuit is connected to supply voltage VDD and the NMOS circuit is connected to ground GND. For the CARRY circuit we can also use an AND gate directly to generate the CARRY signal from inputs. For different input combinations, we can verify the logic using the output waveform.

IMPLEMENTED CIRCUIT DESIGN:



IMPLEMENTED WAVEFORM:



REFERENCE:

• N. H. E. Weste and K. Eshraghian, "Principles of CMOS VLSI design," Addison Wesley, 1993.

• Ishika Sharma and Rajesh Mehra. Delay Analysis of Half Subtractor using CMOS and Pass Transistor Logic. International Journal of Computer Application, vol. 141, pp. 12–16, May 2016