High Efficiency Half-Subtractor Using AVL Technology

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ABSTRACT:

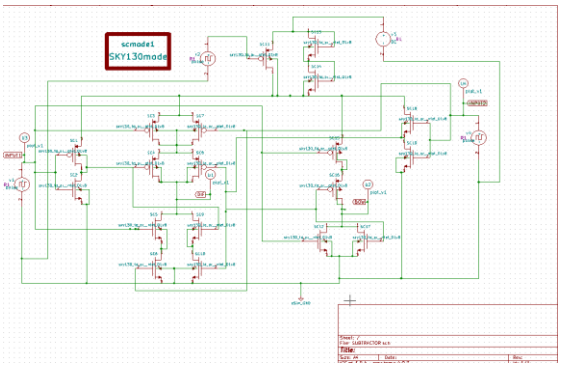
In present day skill, designing of low power systems has emerged as one of the vital theme of electronic industries due to the point that, power consumption and number of components used is drawing much of the absorption in any very large scale integration (VLSI) chip design. Design of low power circuit for high performance is the necessary main concern of VLSI technique. So in this paper, we are going to analyse and conclude the high efficiency half subtractor using various technique. The Adaptive Voltage Level(ALV) technique based Half-Subtractor compared to conventional one based on power consumption, speed, layout area and propagation delay is more preferred.

Keywords-ALV technique, Power consumption, Propagation delay

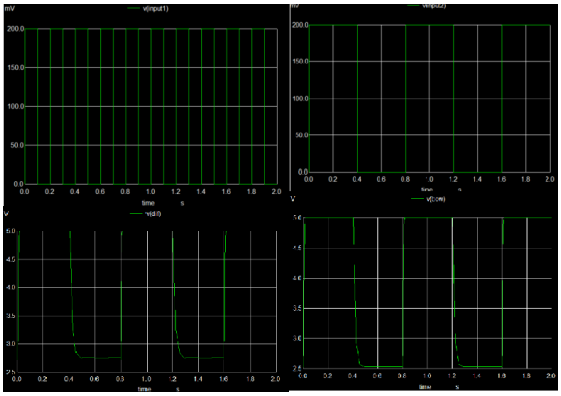
REFERENCE CIRCUIT DETAILS:

In many computers and other kinds of device processors, subtractors are used not only for the arithmetic calculations, but are also frequently used in other parts of the processor, where there is a requirement of calculating addresses, table indices, and similar operations. technology, so lowering the power consumption. In Conventional method, the power consumption and the delay is high as compared to Transistor Level method. As compared to these technique, ALV technique need minimum number of gates, so the delay and power dissipation is very mush less than the CMOS technology. Therefore, ALV technique is the best for constructing the Half subtractor.

DIAGRAM:



OUTPUT WAVEFORM:



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