

Design of 4-bit Servo Tracking type ADC

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Abstract—A 4-bit servo tracking analog to digital converter is designed which can convert analog signal of amplitude ranging between 0 to 8 V. The input voltage VCC of the designed circuit is 9V. For powering flip-flops in counter circuit, 9 V is step down to 5 V using voltage regulator. 4-bit synchronous up down counter is designed using J-K flip flop and logic circuits. The 4-bit digital input is converted to analog output using R-2R ladder type DAC. 555 timer astable multivibrator circuit generates the clock pulses for counter circuit.

Keywords—JK Flip Flop, op amp, 555 timer, DAC, ADC

I. REFERENCE CIRCUIT DETAILS:

Fig 1 shows the circuit of servo tracking type ADC, the circuit contains up-down counter. The up-down counter counts up when the comparator output is HIGH and counts down when comparator output is low. The up-down counter output is in digital format, the output of up-down counter is fed to digital to analog converter which creates a staircase waveform. The staircase wave generated is within 1 LSB of the correct value, provided analog input changes slowly.

Fig 2: shows 4 bit synchronous up-down counter, if the comparator output is HIGH the counter counts up i.e., increase the initial 4-bit data by binary 1 after each cycle. If the comparator output is LOW, the counter counts down i.e., decrease the initial 4 bit by binary 1 after each cycle. Q0 is the LSB of 4 bit up-down counter output, Q3 is the MSB of 4 bit up-down counter output,

Fig 3: shows R-2R ladder type DAC. The Input 4-bit data is of form d1 d2 d3 d4 the data is converted to analog voltage V_o given by $(d_1 2^3 + d_2 2^2 + d_3 2^1 + d_4 2^0) (R_f/R) (V_r/2^4)$. The output wave form is staircase type. d_n is considered as 1 for voltage level V_r . d_n is considered as 0 for voltage level 0. (R_f/R) is decided as per gain requirement of circuit.

Fig 4: shows a astable multivibrator circuit which generates clock pulse for up-down counter circuit. The frequency of astable multivibrator is given by $1.44/([R_1+R_2]C_1)$. The duty cycle will be kept as 50%. Also, Duty cycle is $R_1/(R_1+R_2)$. Clock pulse output is received at pin 3. The output Clock pulse is used for clock in up-down counter circuit.

II. REFERENCE CIRCUIT DESIGN

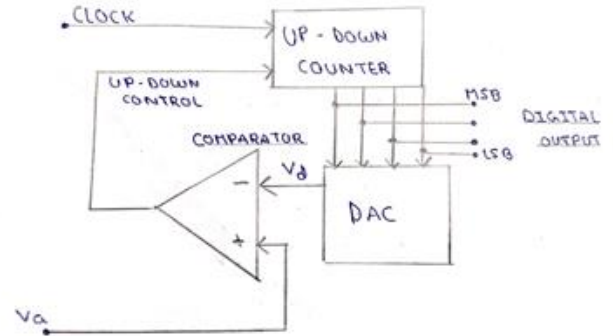


Fig. 1. Servo Tracking Analog to Digital converting circuit

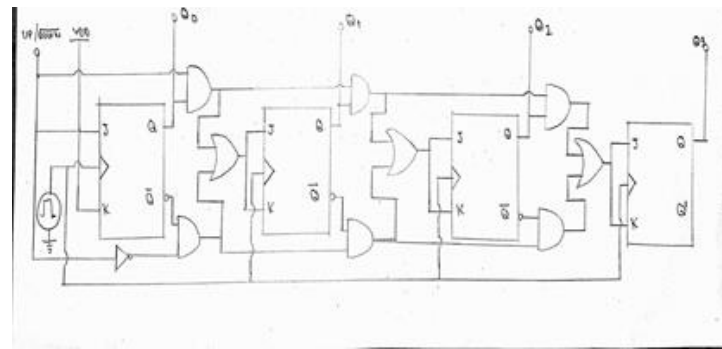


Fig. 2. Synchronous Up-Down Counter Circuit

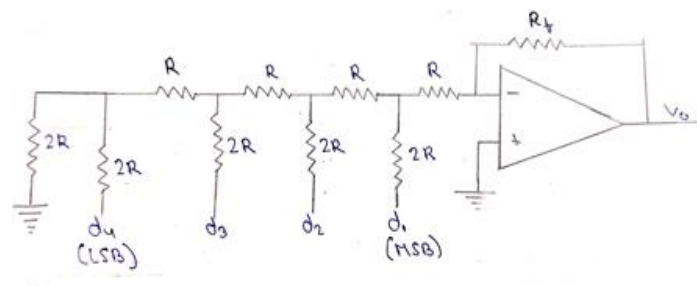


Fig. 3. R-2R type Digital to Analog Converter

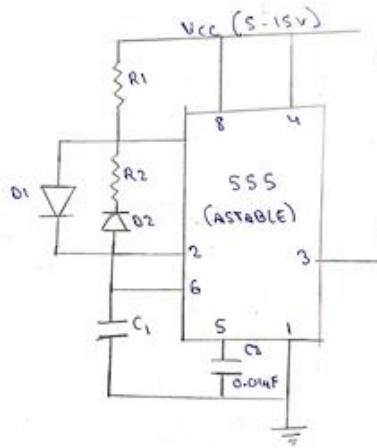


Fig. 4. Astable Multivibrator 555 Timer generate clock pulse

III. REFERENCE WAVEFORM

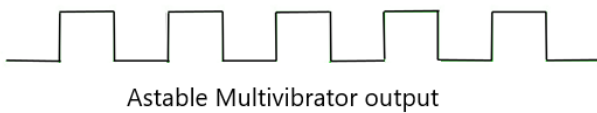


Fig. 5. 555 timer output waveform. Clock pulse

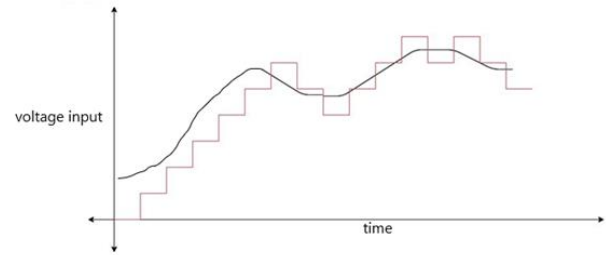


Fig. 6. Digital to Analog Converter output waveform with a input waveform shown above

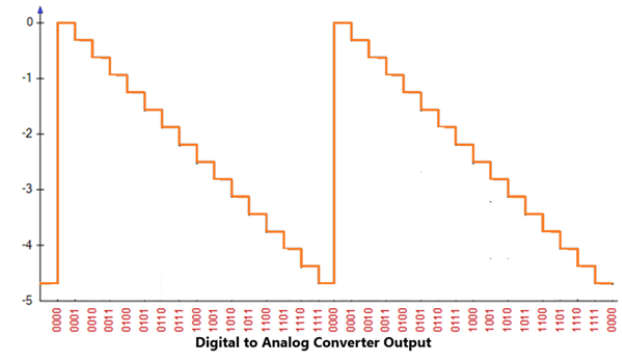


Fig. 7. Digital to Analog Converter waveform output corresponding to 4 bit output data of up-down counter circuit

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