# Design of Master Slave D flipflop with an analog clock circuit

Kishan Pentyala
KL university, Andhra pradesh,
India
kishanpentyala@gmail.com

***Abstract*— This paper presents design of a Master slave D flipflop which works on a level triggered clock. Design is done using esim, Makerchip-Ngveri and sky130 pdk. This design provides stable output irrespective of glitches at input and used as an alternative to negative edge triggered D flipflop**

***Keywords*— Master slave, OPamp, Edge triggered**

## REFERENCE CIRCUIT DETAILS

Fig.1 Shows the Circuit of Master Slave D flipflop in eSim. The Master slave block is a digital block and made using Verilog code in Makerchip-Ngveri tool.

Here a ring oscillator and a Schmitt trigger circuit is used to generate an analog clock wave and given through ADC to Master slave D Flipflop. 3stcmringosci13 and smttrigger21 are the Analog sky130 IPs from FOSSE eSim-IP-Library.

Fig.2 We can see clk signal has a period around 60ns and it has active high reset. The circuit becomes active at negative edge of clock, so Master slave flipflop working on level trigger clk act as negative edge triggered D Flipflop.

## CIRCUIT DIAGRAMS AND WAVEFORM

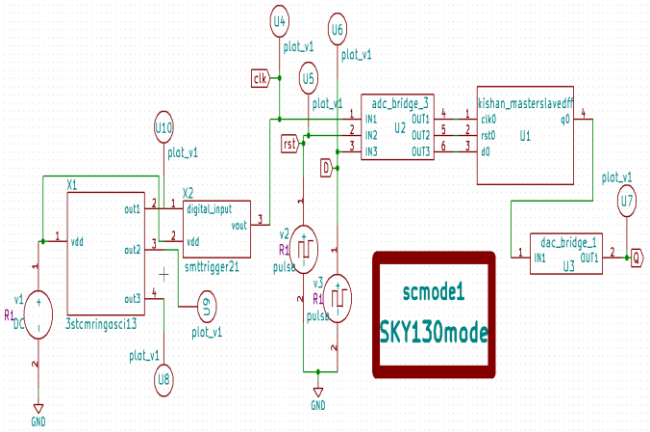


**Fig1: Implemented Circuit diagram**

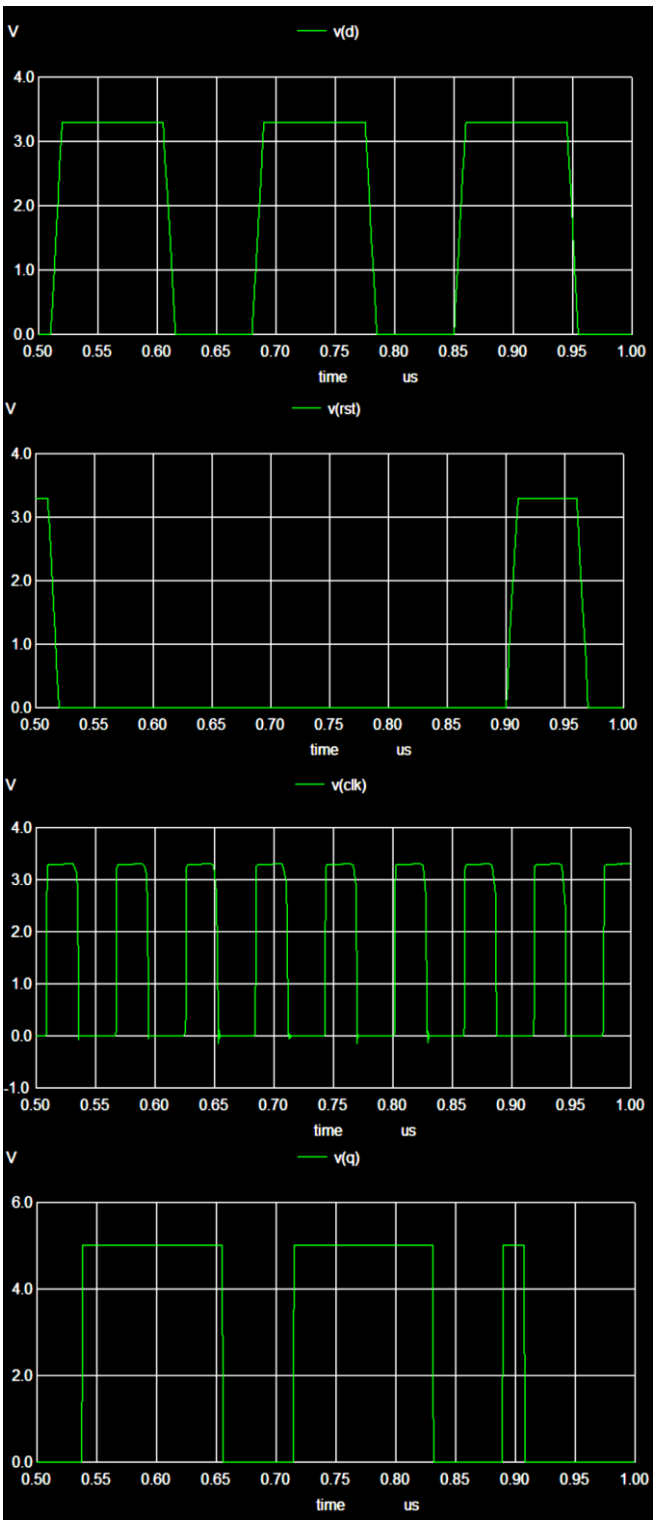


**Fig2: Waveforms**

## REFERENCES

1. Behaviour of Master slave DFlipflop
2. Analog Sky130 IPs from FOSSE eSim-IP-Library