DFSK DEMODULATION

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Abstract **-** DFSK Demodulator is proposed in this paper for achieving high power-transmission efficiency, high data transmission bandwidth. A clock regenerator present in the circuit is used to block squares up the sinusoidal carrier across the receiver and feeds it into the data detector block.

Keywords: Clock regenerator, Digital Block, Ring Oscillator, 3-bit Counter.

I. Reference circuit details

In a digital approach of DFSK demodulation, the duration of carrier cycle is measured with a constant frequency clock time-base at a rate several time higher than the carrier frequencies. An n-bit counter runs while the carrier is 'positive' and measures half of a carrier cycle. When the carrier goes 'negative', the counter stops, and a digital comparator decides weather a long or short carrier cycle is received by comparing the count value with a constant reference number.

It has the Advantages of lower probability of error, provides high SNR (Signal to noise ratio), Simple implementation, Operate in virtually any wires available and DFSK has High data rate.

II. Circuit diagram

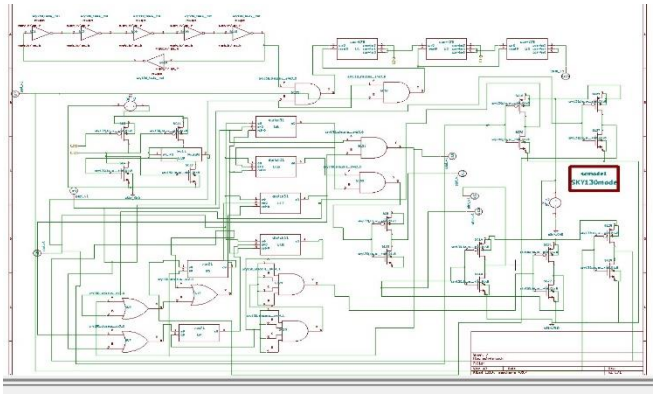

Figure 1. DFSK Demodulator

III. Output Waveform

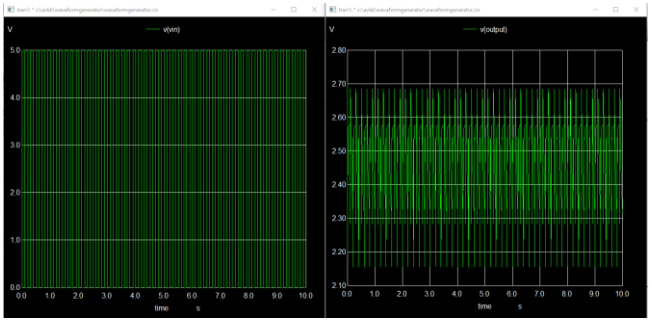

Figure 2. Output wave form of DFSK demodulator

IV. References

[1] Ghovanloo, Maysam, and Khalil Najafi. "A wideband frequency-shift keying wireless link for inductively powered biomedical implants." *IEEE Transactions on Circuits and Systems I: Regular Papers* 51, no. 12 (2004): 2374-2383.

[2]https://youtu.be/rrgon8Qne_E

[3] https://youtu.be/wdb_aZqo7cI