Design and Analysis of Pass-Transistor XOR Gate

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Abstract

The growth of the electronics market has driven the VLSI industry towards very high integration density and system on chip designs. The more popularity of portable electronics is driving designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. The XOR circuit is one of the basic building blocks of many arithmetic and encryption circuits. This paper is proposed to implement a low-voltage CMOS 2-input pass-transistor XOR gate. This design aims to minimize power dissipation and reduce transistor count while at the same time reducing the propagation delay.

1. Reference Circuit Details

A low-power constrained 2-input XOR gate is proposed which is based on pass-transistor logic with an inverter as the output driver to obtain a perfect output swing. The use of pass-transistor design reduces the transistor count along with smaller input loads thus resulting in a very low-power operation with high performance. As a NMOS device passes a strong "0" but a weak "1" while a PMOS device passes a strong "1" but a weak "0" so the complementary pass transistors will pass a strong output logic level for all input combinations of "1" and "0". To drive a full-rail output of "1", V_{DD} connects to the source terminal of transistors M_3 and M_4. When A=0 and B=0, the transistor M_3 is ON, passing a strong "1" from V_{DD} to the inverter input which generates a "0" at the output Y to turn ON the M_4 transistor. When A=0 and B=1, the transistors M_2 and M_3 are ON which passes signals "0" and "1" respectively. Therefore, we need to increase the W/L ratio of transistor M_2 making it larger than the W/L ratio of transistor M_3 so as to pass only a signal "0" to the inverter and to generate the strong output Y=1. When A=1 and B=0, only the M_1 transistor is ON, and a strong "0" is passed to the inverter generating "1" to output Y. When A=1 and B=1, M_1 and M_2 are ON and a weak signal "1" is passed to the inverter input and thus the output Y degrades. Therefore, the feedback path with transistor M_4 turns ON when Y=0 resulting the perfect signal "1" from V_{DD} to the inverter and thus the perfect signal "0" at Y is obtained.

2. Reference Circuit design

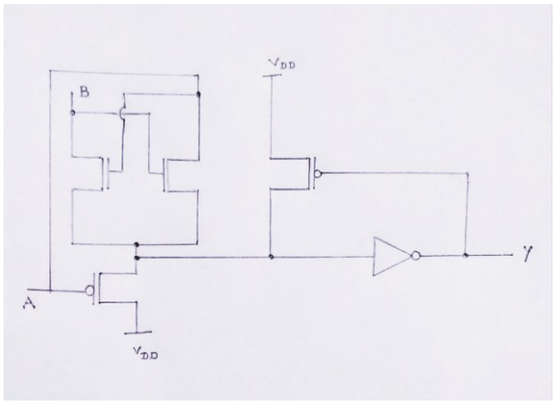

Fig:1 Circuit diagram of the proposed pass transistor-based CMOS XOR gate

3. Reference Circuit Waveforms

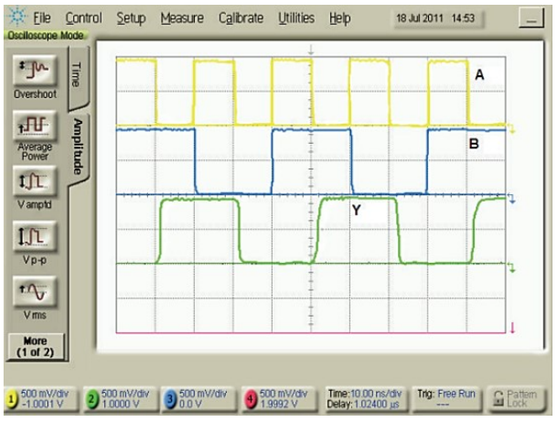

Fig:2 Waveforms for the CMOS pass-transistor-based XOR gate (yellow = input A, blue = input B, and green = output Y).

References

[1] CMOS Digital Integrated Circuits – Analysis and Design by Sung-Mo Kang and Yusuf Leblebici, Third edition, Tata McGraw-Hill.

[2] Nabihah Ahmad and Rezaul Hasan, A 0.8 V 0.23 nW 1.5 ns Full-Swing Pass-Transistor XOR Gate in 130 nm CMOS, Hindawi Publishing Corporation, Volume 2013.