Design of Serializer with LVDS Driver

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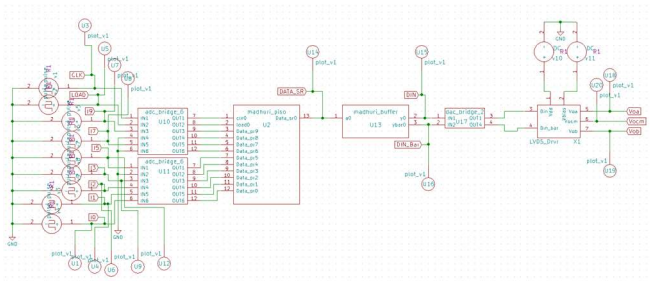
***Abstract*—This paper proposes the implementation of Serializer with Low Voltage Differential Signaling (LVDS) based driver design using CMOS technology with 180 nm Technology. Serializer is a mixed block which uses a Parallel In Serial Out (PISO) Digital Block and LVDS Driver as Analog Block. Serializers are used for High Speed Digital data transmission over a communication channel such as copper cable. It also helps to reduce the no. of ports in multiport operation as multiport parallel data can be multiplexed, serialized with the help of PISO and transmitted over a cable with LVDS Driver. This Mixed circuit will be redesigned and simulated with 180 nm process node using eSim EDA tool developed by FOSSEE IIT Bombay.**

I. CIRCUIT DETAILS

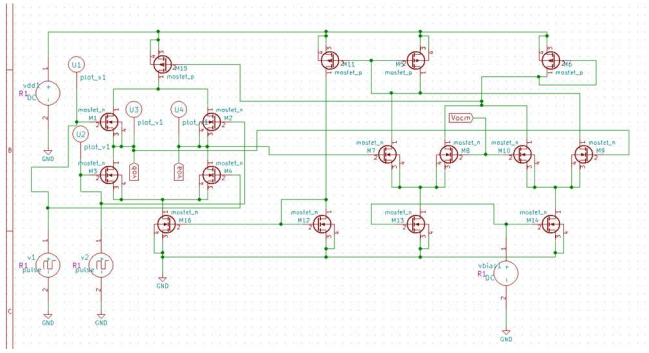
Serializer Block diagram in eSim is shown in section II. It consists of PISO digital Block which will convert parallel data from multiple inputs to the serial bit stream as D_in and Dbar_in. These two are 180 degree out of phase with each other. These opposite serial bit streams are then given to the LVDS driver.

LVDS Driver circuit diagram drawn in eSim is shown in section III. Here transistors M1, M2, M3 and M4 are acting as a current source which are switched ON or OFF based on the input signal polarity D and ~D. The LVDS Driver output is obtained in the form of differential output signals as Voa and Vob which are coupled to 100 ohm transmission line. When D = 1, M1 and M4 will be conducting while M2 and M3 will act as open circuit. This will result into Vob = High and Voa = Low. When D = 0 reverse will occur.

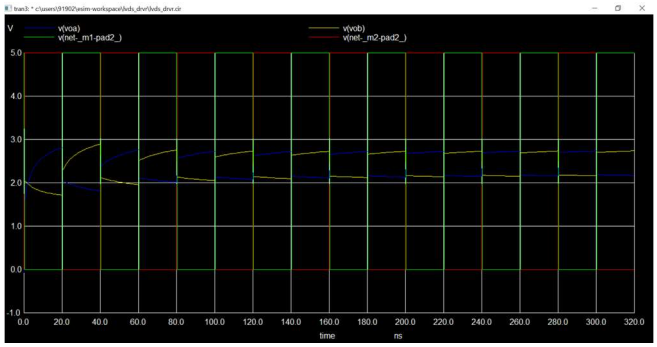
II. SERIALIZER BLOCK DIAGRAM



III. LVDS CIRCUIT DIAGRAM



IV. DRIVER CIRCUIT WAVEFORMS



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