

Half Adder Using Pass Transistor Logic

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Abstract

With the increasing technology, the size of the transistors is reducing. The reducing size leads to the tradeoff between power, efficiency and switching time. Because of which there is requirement to design low power transistor with less area and lesser number of gates. The design should use lesser power as well. Thus, making it more and more efficient.

1 Reference Circuit Details

n-MOSFET is used for implementing Pass Transistor Logic (PTL). Based on the value of control signal n-MOSFET acts as electrical switch. For implementation of any logic gate only few transistors are required if PTL is used.

In this circuit, primary input A is treated as control input. When control input A is applied as logic '0' then transistors N1 and N3 are switched on and behave like short circuits whereas transistors N2 and N4 are switched off and behave like open circuits. Thus, input B is passed to the output line representing sum 'S' and carry output 'C' is obtained as 0 volts, i.e., logic '0'. When control input A is applied as logic '1', then transistors N1 and N3 are turned off and behave like open switches whereas transistors N2 and N4 are turned on and behave like closed switches. Thus, sum output, S is obtained as complement of data input B and carry output, C is obtained as replica of data input B. The input-output waveforms obtained after simulation of the circuit

2 Implemented Circuits

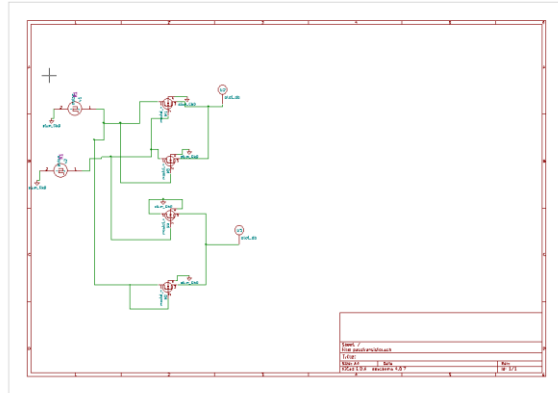


Figure 1: Half Adder Using Pass Transistor

3 Implemented Circuit Waveforms

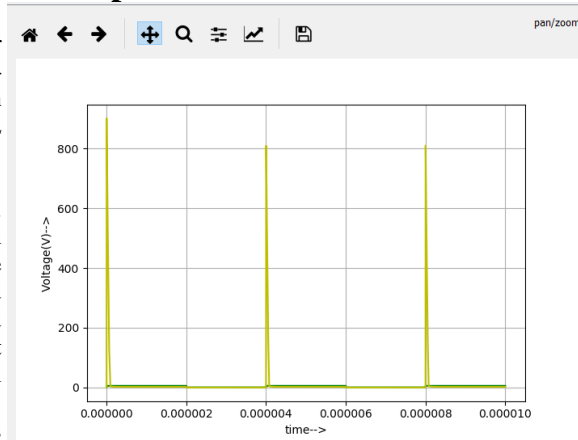


Figure 2: Half Adder Using Pass Transistor Output Waveform

References

1. Rajput, A., Dua, T., Kumawat, R. and Srinivasulu, A., Half Adder Using Different Design Styles: A Review on Comparative Study.