High Speed Dadda Multiplier

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***Abstract*—The speed of multiplier circuits affects the performance of digital systems and so it is very important to develop better algorithms for faster, more efficient processing and Dadda multiplier is one of the fastest ways of implementing a multiplier. It's significantly faster and gate-efficient from the the array multiplier. The objective of this hackathon is to design a NxN Dadda Multiplier circuit.**

***Index Terms*—Multiplier, Performance, Dadda, Algorithms, Array multiplier**

I. Dadda Multiplier

Dadda multiplier[1] is an efficient method of implementing multiplication function, much like the Wallace Tree Multiplier and the Booth Multiplier. There is a lot of considerations that are taken into account while designing these algorithms for better computation purposes. The method of implementing adders as well determine the speed of the design. Dadda multipliers are generally more gate efficient than their Wallace counterparts [2].

II. Methodology of Dadda Multiplier

- Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding N^2 results. Depending on position of the multiplied bits, the wires carry different weights.
- Reduce the number of partial products to two layers of full and half adders. *The tricky part is the reduction method*
- Group the wires in two numbers, and add them with a conventional adder.

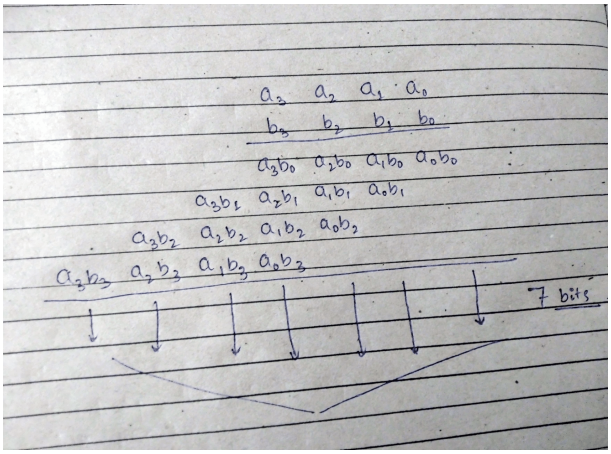

Fig. 1. A 4-bit multiplication method

III. Expected circuit design methodology

We will need N^2 and gates (in this case 16) at the initial stage to implement the basic 2-bit multiplication and then the reduction process starts as shown below.

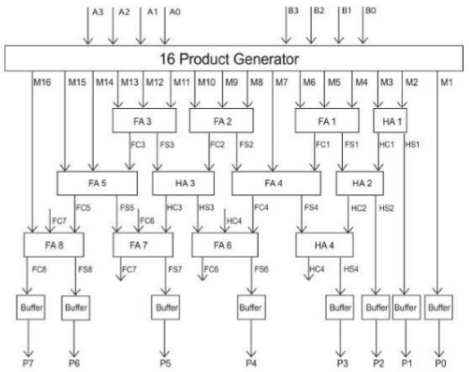

Fig. 2. Design representation

The components like Half Adder(HA), Full Adder(FA),etc. are combined in different stages to help the faster computation of the multiplication output. The delay between the Dadda and Wallace multiplier are same. The complexity of the reduction stage od Dadda multiplier results in smaller number of gates and adders being used.

The Dadda multiplier's speed can be increased by increasing the efficieny of gates but that is to a certain extent only, the other improvement can be usage of look-ahead carry adder or even the improvement in algorithm

References

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[3] Addanki Purna Ramesh, "Implementation of Dadda and Array Multiplier Architectures Using Tanner Tool ," *International Journal of Computer Science Engineering Technology (IJCSET)*