In-Memory DAC Operations Inside 8T SRAM Cells

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***Abstract*— The von-Neumann computing methodology dominates most of the today's processor architecture. In such architecture, program and data are decoupled from each other leading to massive latency as well as energy consumption due to frequent shuttling back and forth of data between physically separate memory and computing cores also known as *bottleneck*. Digital to analog convertor (DAC) is one of the frequently used block inside any processing core which needs to interface analog and digital world. In this paper, we will design an 8T SRAM based in-memory DAC convertor to overcome the von-Neumann bottleneck.**

***Keywords*— bottleneck, DAC, SRAM, von-Neumann**

I. Introduction

Most of the recent day processors works on von-Neumann architecture [1]. In von-Neumann architecture program and data units are spatially, separately stored at different locations on the chip, leads to significantly high delay and energy consumption due to frequent data transfer between physically separated memory and computing cores. This problem is further exacerbated for data intensive applications such as in AI/ML, DSP processors, etc. By enabling computations within memory, significant improvements, both in energy efficiency and throughput are expected [2]. Digital to analog convertor (DAC) is a key block to these applications to interface analog signal with digital processors/algorithms. So, in this work, we will design an in-memory DAC inside 8T SRAM cell.

II. 8T Sram Cell For In-Memory Dac

An 8T-SRAM, without modifying its basic circuit structure, can behave as a digital to analog converter (DAC), without affecting the bits stored in the SRAM cell. Consider an array of 4 cells connected as shown in Fig. 1. Under normal memory operations, the source terminal of M1 (and also M3, M5, M29) is grounded but for DAC operation SLs (source lines) of same row are all connected to *vin*. Thus, the current flowing through each column is proportional to their common *vin*, and also to the conductance of transistors in each of these columns respectively as shown in Fig. 1. e.g., when logic '1' is stored in memory cell of first column, conductance of M1 is very high but when logic '0' is stored in memory cell, the conductance of M1 is almost negligible, i.e., it does not conducts at all. Another parameter on which current will depend is (W/L) ratio of mosfets M1 and M2 present in first column. It is well known that current through enhancement mosfet is directly proportional to its (W/L) ratio. Hence, properly sizing the (W/L) ratios of mosfet M1 and M2 in each column we can obtained our proposed digital to analog converter. For our proposed structure of 8T-SRAM array cells, current I will be sum of currents through RBL of each

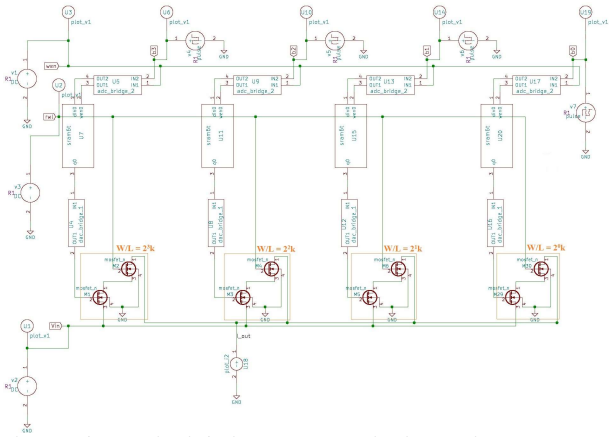


Fig. 1. Reference circuit for in-memory DAC implementation.

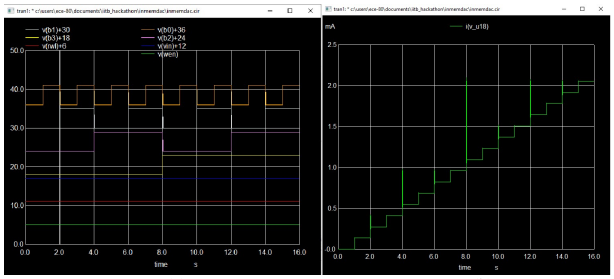
cell. Now consider that the ratio of (W/L) of mosfet M1 and M2 used in column 1 through 4 is 8: 4: 2: 1 as shown in Fig. 1 (we will keep the sizes of mosfet same in each column). Hence, their conductance will be in the same ratio, since conductance will be directly proportional to (W/L) ratio. This will generate output current I, which will be proportional to the analog equivalent of digital bits stored inside SRAM. This will generate output current I, which will be proportional to the analog equivalent of digital bits stored inside SRAM, i.e.,

$$I = K \cdot (2^3 b_3 + 2^2 b_2 + 2^1 b_1 + 2^0 b_0)$$

where, K is some other constant

III. Simulated Waveforms

Fig. 2 below presents the simulated waveforms showing the typical staircase output of DAC.



(a) (b)

Fig. 2. Simulated output showing (a) inputs signal to the circuit, and (b) staircase output current which is typical to the digital to analog convertor (DAC).

References

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[2] S. Jeloka, N. B. Akesh, D. Sylvester, and D. Blaauw, "A 28nm configurable memory using push-rule 6T bit cell enabling logic-in-memory", IEEE J. Solid-State Circuits, vol. 51, no. 4. Pp. 1009-1021, Apr. 2016.