Mixed signal design of Carry look ahead adder

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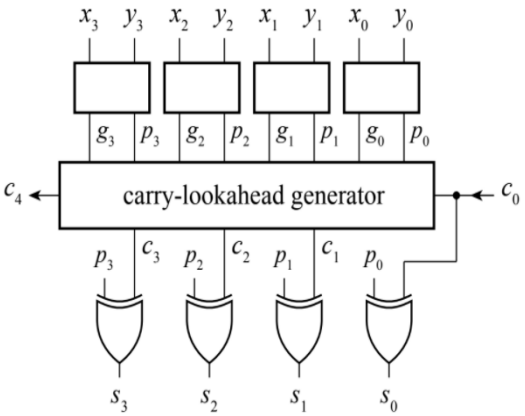
Abstract

This paper proposes the design of 4-bit carry look ahead (CLA) adder using mixed signal design.It has an ADC and DAC block.In the middle we have a digital block consisting of carry look ahead adder.The main advantage of CLA adder is that it computes the carry at all the stages at the beginning itself ,hence reducing the time. While in ripple carry adder it has to wait until each sum output is produced so it causes the delay.

1. Circuit Details

The above circuit has 3 parts , first one is the analog to digital converter which takes analog input and gives the corresponding output to the digital block which has 8 inputs i.e input A of four bits input B of four bits and a carry in .

The digital block is designed using a Hardware Description Language (HDL) Verilog. Along with the adder circuit we design the carry look ahead generator block . The carry look ahead adder produces corresponding sum output and the carry output.The output of the carry look ahead adder is given to DAC ,from which we obtain the final result



2. Implemented Circuit

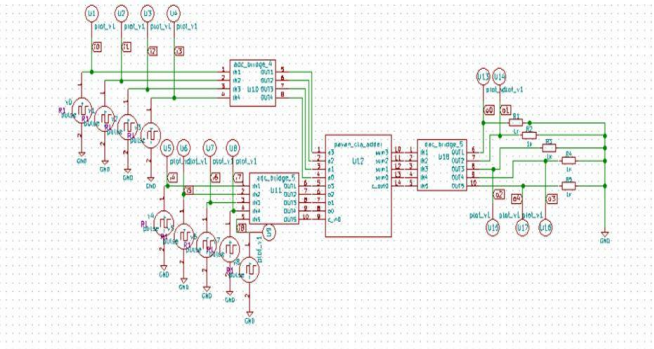
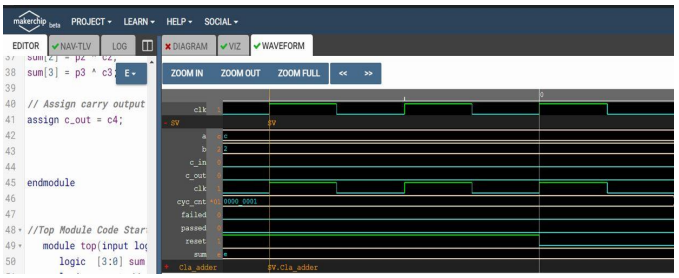


Fig-1: CLA adder using mixed mode design

3. Circuit Waveforms



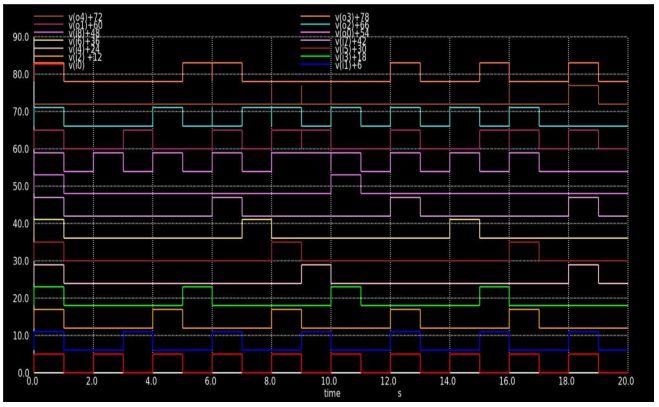


Fig-2: Simulation result of CLA adder

References

[1] Verilog HDL: A guide to design and synthesis by Sameer Palnitkar