8-Bit Digital Sine wave generator

Inderjit Singh Dhanjal, *K.J Somaiya of Engineering, Mumbai*

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***Abstract*- Producing and manipulating the sine wave function is a common problem encountered by circuit designers. Sine wave circuits pose a significant design challenge because they represent a constantly controlled linear oscillator. Sine wave circuitry is required in a number of diverse areas, including audio testing, calibration equipment, transducer drives, power conditioning and automatic test equipment (ATE). Control of frequency, amplitude or distortion level is often required and all three parameters must be simultaneously controlled in many applications with analog and digital approaches. This paper presents detailed design of a 8 bit digital sine wave generator with the help of pseudo-random-sequence (PRS) generator, Look-up table (LUT) and analog low pass filter.**

I. Implemented Circuit Details

The digital block consists of a 8 bit pseudo-random-sequence (PRS) generator running at clock frequency of f_{CLK} = 1.024MHz. PRS generator was written in Verilog code. A PRS output which is finite stream of numbers in the range 1-255 equally distributed was visible clearly in Maker chip plots. A compare function is added, which turns one digital output pin high whenever a value in the shift register (SR) is less the value of the compare input (FE and 80 in hex were chosen). This created a stream of high pulses proportional to the compare value. Next it is fed to Sine wave look up table (LUT), for sine wave generation. LUT code and its functionality was also verified with Makerchip plots. The major challenge was to integrate the two digital blocks, which even two attempts failed to give expected output after integration with analog LPF block.

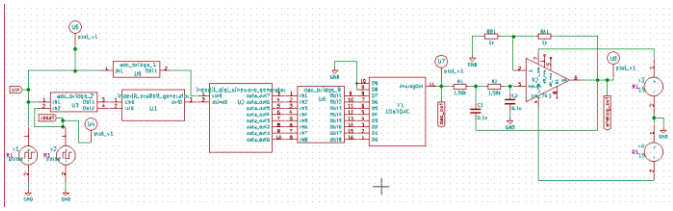

Fig. 1 Digital Sine wave generator schematic (Attempt 1)

In first attempt, the digital block output was fed to a 2nd order low-pass filter designed for a cutoff frequency f_{OUT} = 1 KHz with the help of ADC and DAC bridges as shown in Fig 1 and in next attempt, the digital block output was fed to RLC filter shown in Fig 2. In third attempt, sine wave LUT points were increased from 16 to 256 points.

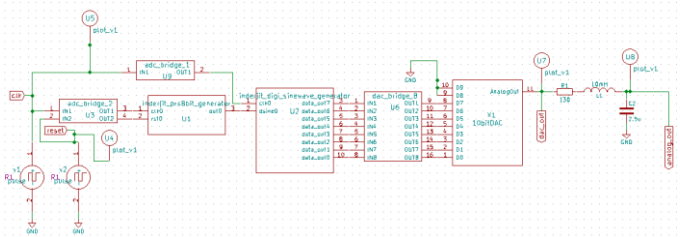

Fig. 2 Digital Sine wave generator schematic (Attempt 2)

II. Implemented Waveforms

Fig. 2, 3 & 4 depicts outputs waveforms at the output of analog low pass filter and DAC output. Three attempts were made to arrive at the expected output which should be a sine wave with 1KHz frequency digitally controlled with input clock frequency of 1.024MHz. The output plots were not as desired.

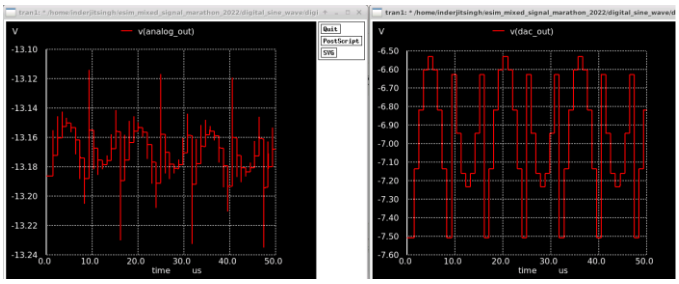

Fig. 2 Output plots (Attempt 1)

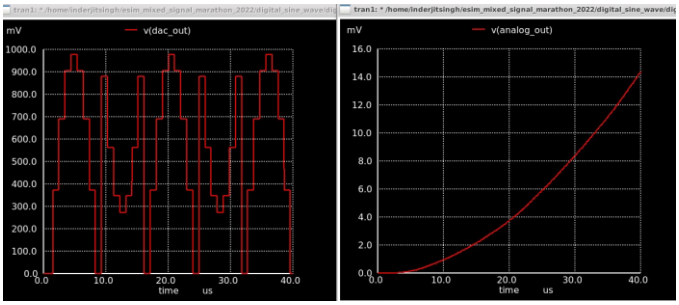

Fig. 3 Output plots (Attempt 2)

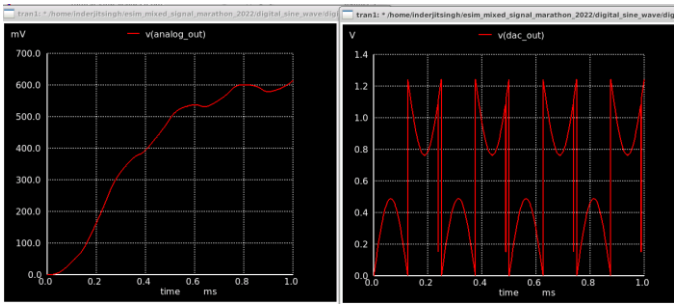

Fig. 4 Output plots (Attempt 3)

References

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