# Design and Analysis of a 2:1 Multiplexer

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## Abstract

The paper constitutes the design and analysis of a 2:1 Multiplexer. Multiplexer is a combinational circuit that has maximum of $2^n$ data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since there are 'n' selection lines, there will be $2^n$ possible combinations of zeros and ones. So, each combination will select only one data input. Multiplexer is also called as Mux. The 2:1 Multiplexer has been designed using CMOS.

## 1 Circuit Details

The given 2:1 MUX has two inputs(I0,I1), one selection input (sel), and one output line(Y). Therefore, it can have only two achievable combinations, i.e., 0,1. When selection input is '0' then input line 'I1' is preferred and is directed to the output, Y. Similarly, when selection input is '1' then input line 'I1' is preferred and is directed to the output, Y. CMOS based 2:1 MUX is a build-up of two sections namely, pull up lattice and pull-down lattice. Pull up lattice is known as PMOS, and pull-down lattice is known as NMOS. In this model, the PMOS device is connected to the supply voltage (VDD) and NMOS is connected to the ground (GND). Both PMOS and NMOS substrate is given to the source terminal (given to VDD in case of PMOS and GND in case of NMOS). From the circuit, if both I1 and I2 inputs are high, then both the NMOS transistors will conduct, neither of the PMOS transistors will conduct, and a conductive path will be established between the output and VDD, bringing the output low. If both I1and I2 inputs are low, then neither of the NMOS transistors will conduct, while both PMOS transistors will conduct, establishing a conductive path between the output and VDD, bringing the output high. If either of the I1 or I2 inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and VDD, bringing the output high.

## 2 Circuit

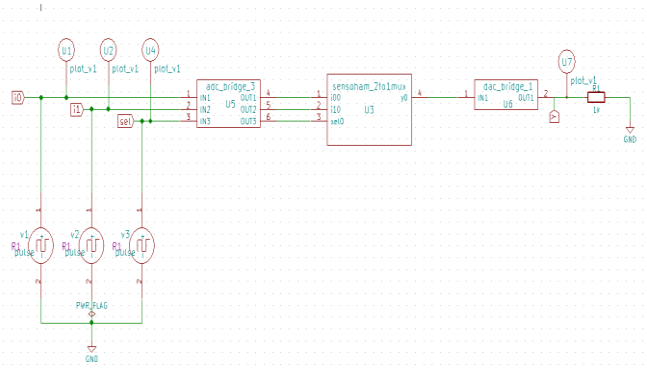


Figure 1: Reference circuit diagram.

## 3 Circuit Waveforms

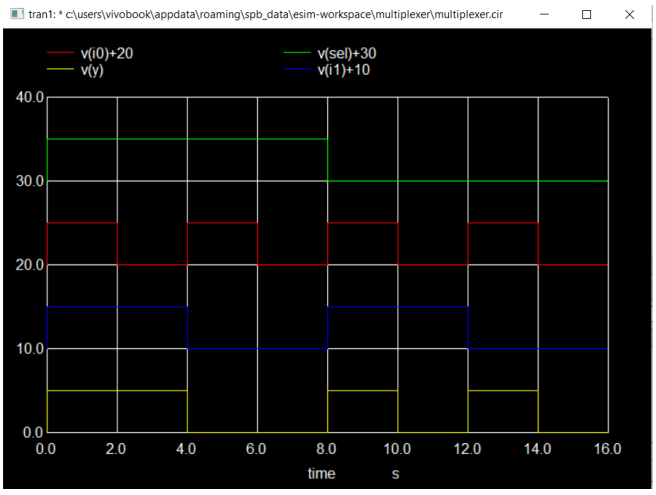


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Figure 2: Reference waveforms

## References

[1] Shyam Sankalp Pattnaik. Design of 2 to 1 Multiplexer in eSIM. https://cutt.ly/UAwYMew.

[2] N. H. E. Weste. Cmos vlsi design: A circuits and systems perspective. https://cutt.ly/InNnZPb.