

Abstract— Analog to digital converter (ADC) is an integral part of communication and an important asset for virtual sign processing. Analog to digital converter (ADC), find a wide variety of applications in today's digitalized world. Flash ADCs are quickest amongst all of the forms of ADCs located so far. A 4bit Analog-to- Digital Converter (ADC) is designed for low strength and low power consumption. It calls for 2N-1 comparators, an encoder to transform thermometer code to binary code.

In this paper, we are going to design a 4bit flash Analog-to-Digital Converter (ADC) to gain excessive-velocity the use of 180nm CMOS technology. The results received also are provided here. The physical circuit is extra compact than the preceding design. The analog output of each comparator depends upon the input, the reference voltage supplied to the priority encoder, and finally, the virtual output obtained. Power, processing time, and region are all minimized. This design may be used for modem excessive-velocity ADC applications. In this, all processes have been carried out of a CMOS based 4bit flash Analog-to- Digital Converter (ADC) using Open-Source Software eSim.etc.

Keyword-eSim tool,

I. INTRODUCTION

Analog to Digital Converters (ADCs) are the maximum essential devices, which connect Analog block with digital block and use everywhere all over the world. ADC is a tool that converts the input Analog amount to digital numbers. ADCs incorporate 3 fundamental parameters, which can't be changed once it has been planned, and the parameters consist of speed, resolution and power dissipation. ADC, which is being mentioned nowadays, requires a structure having low energy dissipation and high velocity of operation. A single structure cannot be used for all of the packages as various varieties of ADCs range from every different on the idea of overall performance parameters inclusive of velocity, power consumption, and decision. Hence, it is extraordinarily essential to select an ADC for each specific application. A distinctive type of ADCs is available like SAR ADC, Dual-Slope ADC, Sigma-Delta ADC and Flash ADC but amongst all these; the maximum commonly applied ADC is the Flash ADC due to its higher trade-off among its overall performance measurements. Flash ADCs are used for applications in which excessive velocity and low decisions are required. Flash ADC has a bank of comparators testing the input signal in parallel, the comparator financial institution output is fed to an encoder good judgment circuit that produces a completely unique virtual code for every voltage range.

II. REFERENCE CIRCUIT DETAILS

The fundamental block diagram of 4-bit Flash ADC is given. It consists of three primary components: resistors, comparators, and encoders. For N-bit Flash ADC 2N resistors and 2N-1 comparator are required. For 4-bit ADC the circuit utilizes $(2*2*2*2)-1= 16-1=15$ comparators and $(2*2*2*2) =16$ resistors. The comparator comprises of wideband and low advantage tiers cascaded together. At excessive frequencies, the low advantage is acquired as it is difficult to acquire excessive bandwidth and excessive advantage at an equal time. Each comparator has a reference voltage that's 1 LSB better than that of the only one below it withinside the chain. An analog voltage is continued to every voltage comparator to evaluate enter voltage with regard to voltages. The reference voltage is created via way of means of the resistive stepping stool circuit and depending upon the correlation made among VIN and the comparator generates Vref, zero and 1 output. If VIN is much less than Vref, the output is 0 in any other case. The output of the comparator is fed to the concern encoder to acquire the digitalized output.

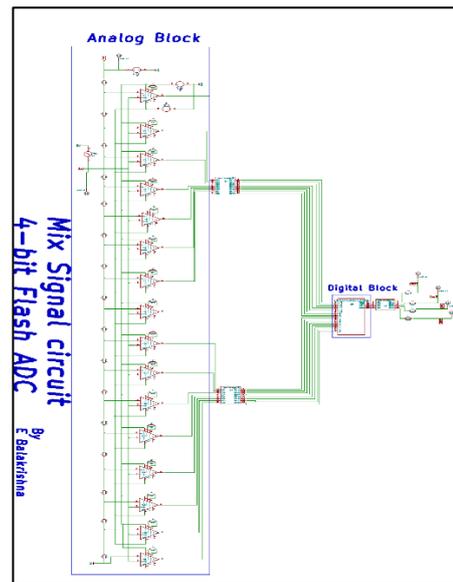
Comparator: Comparator performs an important component withinside the design of Analog-to-Digital converters (ADC). The execution of the goal application is essentially impacted by the design of the comparator.

The velocity and resolution of an ADC are laid low with the enter offset voltage, delay and input signal variety of comparator. The two-level open-loop comparator includes different stages. The first level comprises a differential amplifier and the second level includes an output advantage level as proven in Fig. 1 As this circuit incorporates a minimal quantity of transistors, its circuit area is small.

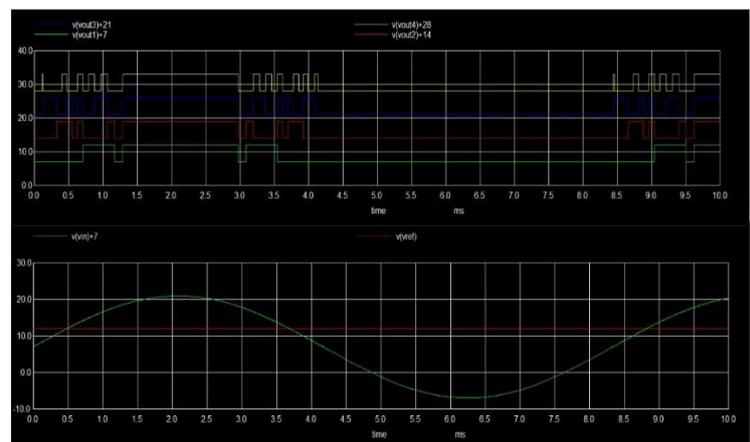
Priority encoder:

- 1) An encoder is used to reduce the quantity of a number of wires wished in a circuit.
- 2)It gives a coded output with the aid of using assigning a priority to the number of bits of input.
- 3)A priority encoder could have a couple of inputs activated at an equal time.

III. REFERENCE CIRCUIT DESIGN



IV. REFERENCE WAVEFORM



IV. REFERENCE PAPER

1. <https://ijeat.org/wpcontent/uploads/papers/v2i2/B0932112212.pdf>
2. https://www.ripublication.com/ijems_spl/ijemsv8n1_05.pdf
3. <https://www.iosrjournals.org/iosr-jvlsi/papers/vol4-issue6/Version-1/G04614146.pdf>
4. <https://research.ijcaonline.org/volume61/number11/pxc3884802.pdf>