UNIVERSAL FLIP FLOP
D FLIP FLOP

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FEB 28, 2022

Abstract

In real life , we have different components for flip flop and latches but think if all these function will be got in single chip? .In this article we are going to design Universal D flip flop which has the capability of level trigger , positive and negative edge triggering according to user's preference.

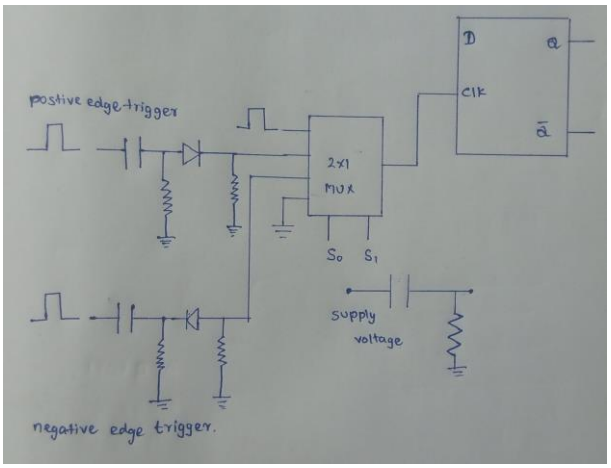
1 Reference Circuit Details

In the circuit, there are three main components such as multiplexer, integrator and D flip flop. 2 x 1 multiplexer is used for circuit implementation. The main idea of the circuit is that the clock of D flip flop is driven by the multiplexer which has the inputs from integrator. Integrator is implemented using resistor and capacitor as shown in figure. The select lines of multiplexer can select the triggering type of flip flop which is shown in below table

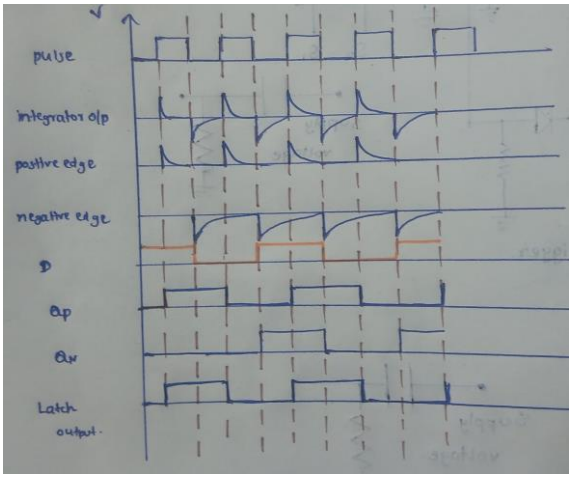
S0	S1	Triggering type
0	0	Level trigger
0	1	Positive Edge Trigger
1	0	Negative Edge Trigger
1	1	Memory

We can implement this method, for other flip flop also by replacing D flip-flop.

Reference Circuit



Waveforms



References

1.https://www.javatpoint.com/verilog-d-flip-flop