An Energy Efficient And High Speed Double Tail Comparator Using Cadence EDA Tools

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Abstract— Comparator is the vital building block of analog to digital converter. The need for energy efficient and high speed analog-to-digital converters is necessary for the use of dynamic regenerative comparators to improve speed and efficiency of power. Fast ADCs, such as flash ADCs, requires an energy efficient comparator with small chip area. In this work comparison is performed among the delay of single Tail comparator, Double Tail Comparator and double tail comparator for less power theoretically and practically. The sub threshold leakage of transistors has usually been very small in the off state, as gate voltage is below threshold. The leakage from all sources has increased as the technology scales down. But as voltages have been scaled down with transistor size, sub threshold leakage has become a considerable factor. Fast comparators in CMOS having the problem of less rail voltages when threshold-voltages(Vt) of the devices are not scaled at the same speed as the rail voltages of the latest CMOS techniques. The proposed work consumes less power about 290mW compared to other types of comparators. The delay for the proposed architecture proved to be 10 ns which is less compared to the other comparators.

Keywords—Comparator, ADC, Threshold leakage, Double tail comparator, Cadence.

I. INTRODUCTION

In Efficient analog to digital convertors , clocked regenerative comparators are very much useful. They can make decisions quickly as they have good regerative feedback in the regenerative flipflop[1][2]. Different analyses such as noise, offset,random decision errors and white noise are present in this work. Here, a delay analysis is presented. The delay of different clocked comparators such as single tail comparator, double tail comparator and double tail comparator for low power is analyzed both theoretically and practically.For each modification in the circuit the delay and power will be reduced[3][5].

The comparator design is modified for the reduction of the leakage power which further reduces the total power and delay of the circuit. The simulation results show the reduction in power and delay. The delay of each comparator will be analyzed. The delay of clocked comparators was analyzed and equations were derived. An Energry efficient and high speed Dynamic comparator latch was designed and it is proved to be outperforms than the previous comparators[7]. A CMOS inverter based amplifier design was implemented to reduce the sub threshold leakage.

This work is organized as follows: Section I covers introduction, section II reveals related work, section III introduces proposed work, section IV depicts the results and section V states the conclusion of the work.

II. REVIEW OF PREVIOUS WORK

A. SINGLE-TAIL COMPARATOR

The basic requirement for Analog to Digital Converters is the dynamic comparator. This comparator has large input impedance, power supply rail to rail output voltage swing and it doesn't offer any static power consumption[8][10]. The circuit mainly operates in two phases, reset phase and decision making phase .This phase depends on the clock input given. The schematic diagram of dynamic comparator is as follows,

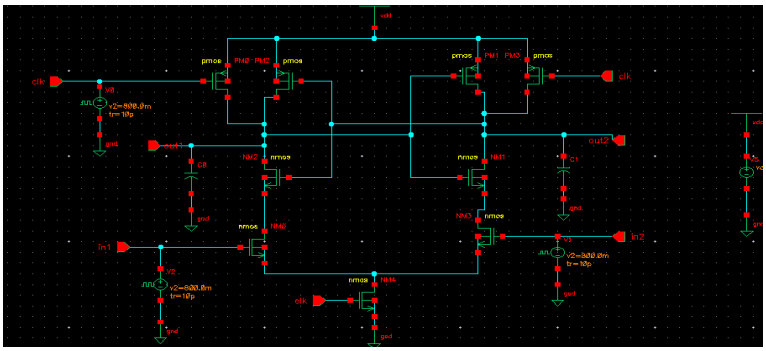

Fig. 1 Single Tail Comparator

A. Operation

During the reset phase, when clk1=0, clk2 is off and both the reset transistors p3 and p4 are on and pull both the output nodes out1 and out2 to V_{DD} which indicates a start condition having a valid logic level in the reset phase[3]. During comparison phase, when clock= V_{DD}, the MOS transistors P3 and P4 are turned-off, so that the out1 and out2 nodes starts discharging with different rates depending on the applied inputs in1 and in2. Assuming IN1>IN2, since the transistors are of same size, n4 transistor will turn on faster than n3 so that output1 discharges faster rate than output2. When output1 discharges to V_{DD}-|Vthp|, the corresponding pmos transistor p1 turns on pulling output node to power supply rail V_{DD}. Thus the regenerative latch which is caused by back to back inverters starts on. Thus, Output2 will be pulled back to V_{DD} and Output1 will be discharged to gnd. If Vin1 <Vin2, the circuits will works vice versa.

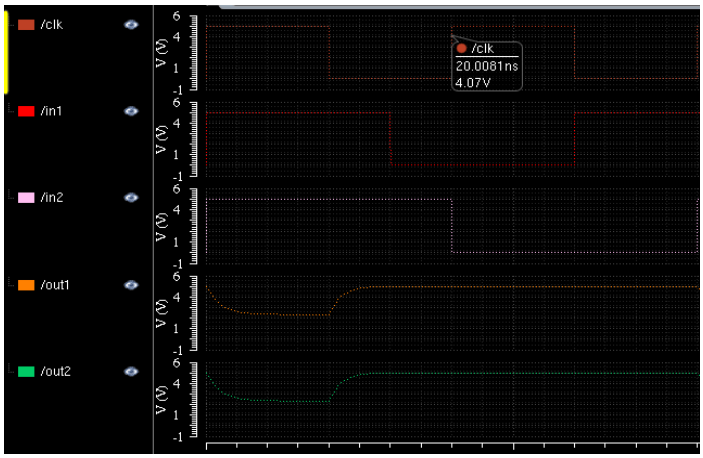

Fig. 2 Single Tail Comparator Simulated Results

The delay of the single tail comparator is calculated as follows

$$tdelay = t0+tlatch \quad \text{-----(1)}$$

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \quad \text{----(2)}$$

The experimental results specifies that reducing the common-mode input voltage along with the increase of t0 and reducing of the tlatch finally this leads to an increase in the total delay of the comparator. This circuit has the benefit of large input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise [6][7]. Here, input transistors parasitic capacitances does not affect the output nodes' switching speed. Hence, to minimize the offset, design of large input transistors is required. On the other side, there is a problem with this topology due to transistors. A large rail voltage is required to obtain a proper t_{delay}. The t_{delay} of the circuit becomes large due to lower g_m of the latch. The main drawback of this circuit is that there is only one path for the current flow. One should prefer a small current path for the differential amplifier to maintain the differential amplifier pair in weak inversion and to get a long integration interval. A high current path is required for the fast regenerative latch.

B. DOUBLE-TAIL COMPARATOR

A double-tail comparator is shown in Fig.3. As compared with the previous structure, this Comparator has less number of transistors, and also can be operated at low supply voltages[4].

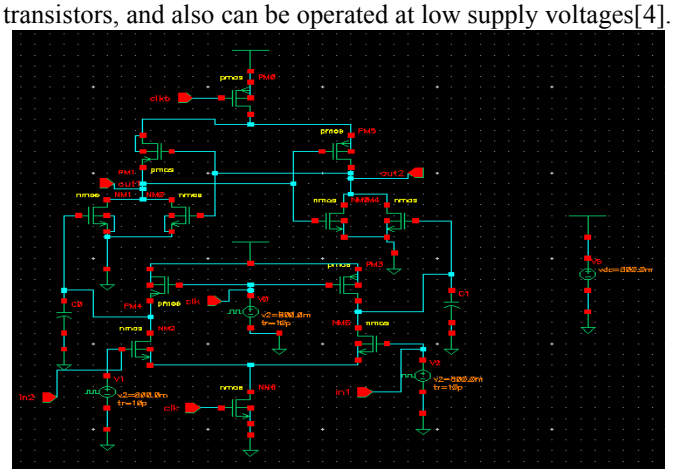

Fig. 3 Double-Tail Comparator schematic diagram

i. Operation

During reset phase, CLK = 0, thus the two tail transistors P0, and N0 are off, and the transistors p1 and p2 are on so that the two nodes fn and fp will be pre charged to V_{DD}, thus the two transistors N1 and N2 discharges the output nodes to gnd. During decision phase CLK=V_{DD}, the transistors mtail1 and mtail2 will be turned on, and both the PMOS transistors p1 and p2 will be turned-off and the voltages at points Fn and Fp begins to drop with different rates[5][6]. The discharging rate at which the voltage drops will be defined by Imtail1/Cfn(p) and therefore differential input voltage ΔVfn(p) will setup.

The two transistors N1 and N2 passes this differential voltage $V_{fn(p)}$ to the latch. The intermediate transistors also provide a enough shielding between input and output which results in the reduction of kick-back noise.

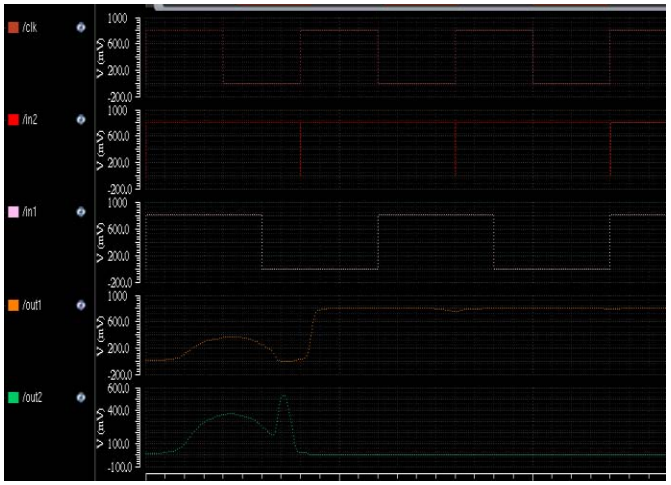

Fig. 4 Double Tail Comparator Simulation Result

The total delay of this comparator can be derived as,

$$t_{delay} = t0 + tlatch \quad \text{------(3)}$$

$$= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}\cdot I_{tail2}^2 \cdot C_{L,fn(p)}}{8V_{Thn}^2 \cdot C_{Lout} g_{mR1,2} g_{m1,2} \Delta V_{in}}\right). \quad \text{---(4)}$$

the summary for the above equations derived for the double-tail dynamic comparator as given below.

a) The differential output voltage will be affected by the voltage difference at the first stage outputs (ΔVfn/fp) at time t_0. The delay of the comparator will reduces by increasing V_{DD}.

b) Both intermediate transistors will be cut-off , so the said transistors will not contribute in improving the effective g_m of the Latch. On the other side, during reset phase, the nodes fn and fp charged from gnd to V_{DD}, which indicates consumption of power.

III. PROPOSED WORK

A. DOUBLE-TAIL COMPARATOR FOR LOW POWER

The diagram of the dynamic double-tail comparator for low power is shown in fig 5. This comparator is designed mainly based on the double-tail structure due to the better performance of double-tail architecture for its low-voltage application. The two control transistors are added to the first stage in parallel to P1/P2 transistors but are in cross-coupled manner to increase the speed of the latch.

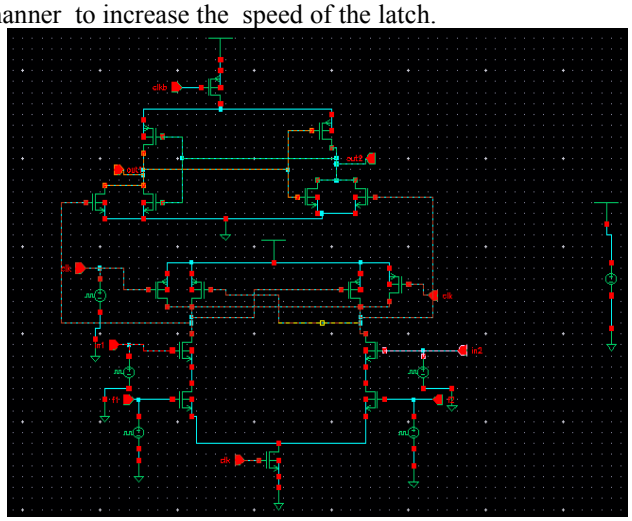

Fig 5. Schematic of Double tail Comparator for Low Power

i. Operation

The working of Double Tail Dynamic comparator is explained below. In reset phase, CLK = 0, N3 and N4 are off, P1 and P2 pulls then both fn and fp nodes to V_{DD}, hence transistor Pc1 and Pc2 are in cut -off region.

Intermediate stage transistors, NR1 and NR2, bring both latch outputs to gnd[6][7]. In comparison stage transistors P1 and P2 turns off. Moreover, at this phase, the control transistors are cut off . Therefore, according to the input voltages, fn and fp reducing at different rates. Consider IN1 > IN2, then fn drops faster than fp, since N1 provides more current than N2. When fn falls below the threshold voltage, the corresponding PMOS control transistor Pc1 starts to turn on, pulling fp node back to the V_{DD}; thus another control transistor (Pc2) remains cut off, makes fn to be discharged to gnd.

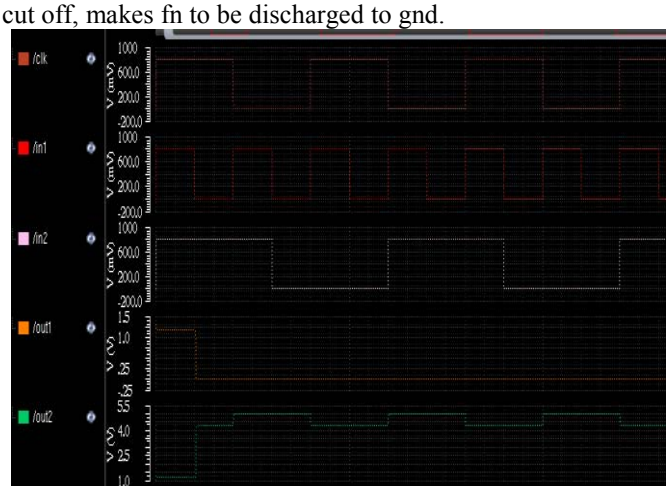

Fig. 6 Double tail Comparator for Low Power Simulation results

fp and fn difference increases in an exponential way, which reduces latch regeneration time. Static power consumption can be obtained by drawing a current from power supply rail (V_{DD}) is drawn to the gnd through input and tail transistor [8][9]. To avoid this, two nmos switches are introduced below the input transistors. The difference in voltage can be increased when the comparator identifies that one of the Fn/Fp nodes is discharging at a high speed. Let Fp is connected to the power supply rail (V_{DD}) and Fn should be completely discharged, the switch to fn closed for the discharge of node. There fore control transistors will functioning as a latch. The delay of the improved comparator is obtained from

$$t_{delay} = t0 + tlatch$$

$$= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \times \ln\left(\frac{V_{DD}/2}{4V_{Thn}\left|V_{Thp}\right|\frac{g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,fn(p)}}\right)}\right).$$

----------(5)

The above expressions were compared for the delay of the three mentioned structures, we can say that the comparator with positive feedback in double-tail operation proved to be an efficient structure. This speed improvement can be observed more in lower supply voltages. Because for higher values of

V_{Th}/V_{DD}, the trans conductance of the transistors decreases, then the existence of an inner regerative feedback in the circuit of the stage-1 will resulting an improved an efficient comparator circuit.

B. SUB-THRESHOLD CONDUCTION

Due to scaling down, the size of transistors has been shrinking. The number of components on chip has been increased to improve the performance of circuits[10].To maintain the dynamic characteristics of an MOS device, the V_{DD} is reduced. Therefore the threshold voltage is also scaled down at the same pace as V_{DD} in order to achieve the transistor switching speed. As a result, leakage currents increases with each technology. As the leakage current increases , the total power dissipation also increases.

$$P_{LEAK} = I_{LEAK} * V_{DD} \quad \text{-------(6)}$$

To reduce leakage current in MOS circuits, some new techniques needed to be developed to reduce the sub threshold leakage especially for chips that are used in portable systems . The sum of reverse bias diode current and Sub-threshold current is same as the leakage current. The current in the reverse bias mode is resulting due to the stored charge between the drain and body of transistors while the Sub-threshold current is due to the carrier diffusion between the drain and source of the transistors. Hence, in this paper conventional CMOS inverter based approach is used to reduce the Sub-threshold leakage power.

C. DOUBLE-TAIL COMPARATOR WITH REDUCED LEAKAGE POWER

The amplifier circuit is modified according to the inverter logic. The inverter logic which reduces the

leakage . Here, two inverters are used. The inputs are applied to two inverters and the outputs are connected[7].

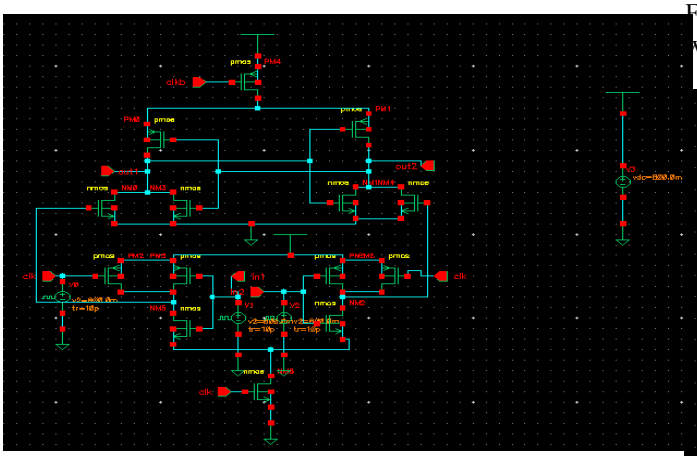

Fig. 8 Double Tail Comparator with Reduced Leakage Power Schematic diagram

i. Operation

In the reset-phase, when Clock=0, p0 & p1 are cut-off and P1 and P2 are on so that the two transistors N1 and N2 will be on and pulls the two output nodes out1 and out2 to zero potential.

In decision- phase, when Clock=positive power supply(V_{DD}), the two tail transistors p1 and p0 are on and P1 and P2 are off which turns the two transistors N1 and N2 off. Consider the case where IN1>IN2, then the transistors N2 will turn on faster so the output of that inverter falls down which turns the intermediate transistor N1 off. Hence, out1 pulls up to V_{DD}. When out1 goes to V_{DD}, the transistor p3 will be off which remains out2 at ground. By using this approaches the Sub-threshold leakage and hence the total power will be reduced.

The simulation results prove the reduction. Here in the differential amplifier inverters are used which are series transistors. Hence, the trans conductance of the total circuit increases which reduces the total delay of the circuit. Hence, by using this CMOS inverter approach the total power and delay can be reduced.

IV. RESULTS

The simulation results of Double Tail Comparator with Reduced Leakage show in fig9.Which shows the reduction in both power and delay.

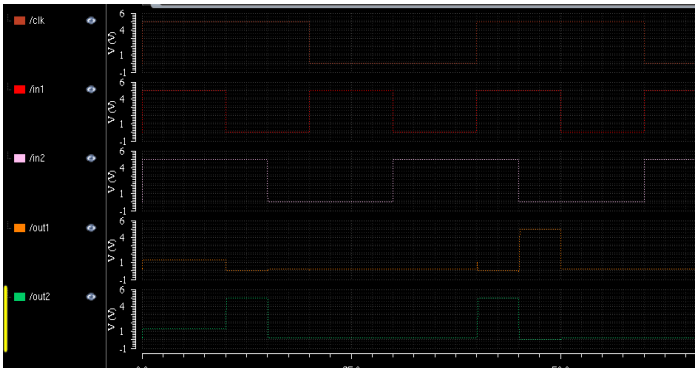

Fig9. Double Tail Comparator with Reduced Leakage experimental Results

Fig. 10 depicts the proposed Double Tail Comparator layout with Reduced Leakage.

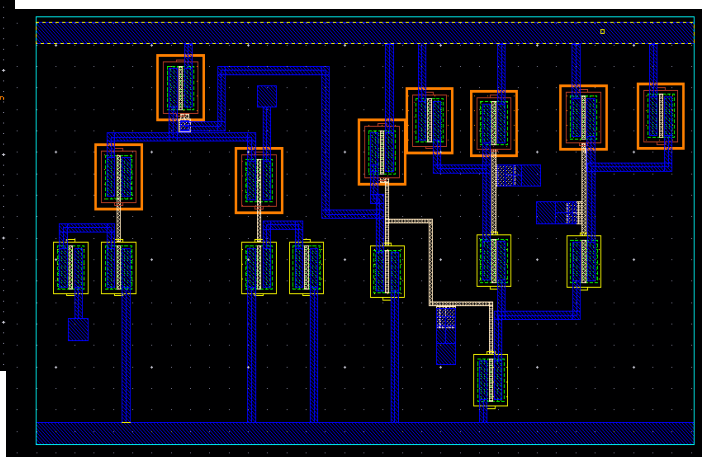

Fig. 10 Layout of Proposed Structure

Table 1 shows the comparison of results among various types of comparators. The proposed work shown to be an energy

efficient and high speed design compared to existing comparators.

Table 1: Results for comparison

Comparator structure	Single-tail comparator	Double-tail comparator	Double-tail comparator with low power	Double-tail comparator with reduced leakage(Proposed)
Technology	180 nanometer	180 nanometer	180 nanometer	180 nanometer
Power Supply voltage	0.8 Volts	0.8 Volts	0.8 Volts	0.8 Volts
Power(mW)	480	530	350	294
Delay	20ns	14ns	12ns	10ns

V. CONCLUSION

The delay of clocked comparators was analyzed and equations were derived. An Energy efficient and high speed dynamic latched comparator was designed and compared with the previous comparators. The experimental results shows that the proposed circuit can operate as an energy efficient and high speed design. Compared to the conventional structure, the proposed method occupies less chip area. A CMOS inverter based amplifier design was implemented to reduce the sub threshold leakage. The experimental results shows that in the proposed work both power consumption and delay are drastically minimized even in small supply voltage. The Power and delay of each circuit were measured and compared. Now we can conclude that the proposed comparator is delay efficient, power efficient and area effective also.

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