Design of a low power, high speed double tail comparator

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***Abstract*—In the fast moving digital world, it becomes imperative to constantly come up with innovation in digitization. The analog to digital converter is the second most widely used device in the world of electronic circuits.ADCs are composed of dynamic comparators. To overcome the challenges faced due to the digital change, improved versions of the conventional comparator design for high-speed functioning and low power consumption has been proposed. Area is another main factor when keeping in mind the design of these dynamic comparators. 180 nm CMOS technology and a constant supply voltage of 0.8V have been used. A conventional double tail comparator has been designed by adding transistors without hindering the functionality. This provides faster, more efficient modification of the comparator design. A new design for a dynamic regenerative double-tail comparator has been proposed which uses clock-gating techniques. This further reduces the power consumption and provides higher speed by reducing the delay time of the circuit.**

Keywords—Comparator; Analog to digital converter(ADC); dynamic comparator; regenerative comparator; clock-gating.

I. INTRODUCTION

A comparator is a decision making electronic device that uses an operational amplifier having a high gain. A comparator compares an input voltage level with another voltage level or a preset voltage V_{REF}. It produces a binary output depending on which analog input voltage is larger. Dynamic regenerative comparators are used to begin with, dynamic signifies the addition of clocks to the input of the circuit design. The outputs are produced depending upon the state of the clock. Regenerative comparators are those comparators using positive feedback like a latch to compare the signals. The feedback aids in providing higher speed in the circuit.

In a comparator, when the non-inverting terminal is at a higher voltage potential than the inverting terminal, the output is pulled up to $+V_{sat}$as shown in the Fig 1. Similarly when the inverting terminal is at a higher voltage potential than non-inverting terminal, the output is pulled down to $-V_{sat}$.

The comparators are most widely used in analog to digital convertors like the flash ADC. The comparator design has a predominant influence on the overall performance of ADCs. For any comparator a low supply voltage, high speed and small chip area is a must. Compensation on the area of the design for achieving the desired high speed and low power becomes inevitable. Hence there exists a trade-off between area and speed of the comparator.

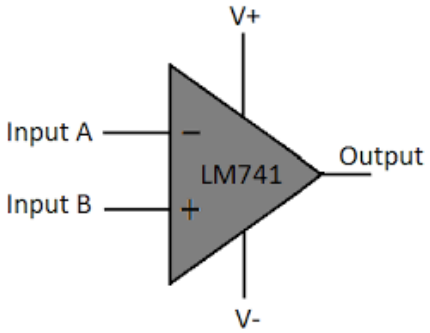

Fig 1. Operational Amplifier in open loop (comparator)

There are three main stages in a comparator; the first stage is the pre-amplifier stage. In this stage the input signal which is fed to the comparator is being amplified. The second stage is a positive feedback stage. This is mainly used to identify the input signal which is high or low. The final stage is the decision making stage and an output buffer stage. Here the main purpose of buffer is to amplify the information which is obtained and produce a digital signal as its output. Designing a comparator is done by considering input common mode range, power dissipation, propagation delay and area of the entire chip.

The implementation of comparators with 4 stages and integrated inductors was done. This used a 10GHz 4-stage comparator in 0.11μm/1.2V CMOS, which was used to obtain every 4th bit of the data stream. With supply voltage being 1V at the input side, a bit error rate of $< 10^{-12}$ was achieved [3].The comparators are used under very low supply voltages

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with help of supply boosting techniques which are based on the usage of static, dynamic and switched voltage sources [4].

The circuit in [3][4] was further modified and the delay time of the comparator was measured with the help of an additional on-chip circuit and the delay time variation of the comparator was found to be σ≈11ps [5].

In [2][3][5] additional circuit has been added to the comparatorso as to improve its speed under very low supply voltages. The modified comparator in [2] works under a lowsupply voltage of 0.5V thereby consuming only 18μw power. Even though the approach is effective the mismatch of components in the added circuit on performance needs to be taken into account.

The structure of double-tail comparator which was proposedin [9] is actually based on designing withtwo stages. The input and the cross coupled stages which are separated. Due to this separation the comparator is able to perform at much faster rate over a variety of common-mode voltage and a wide range of supply voltage [9].In the paper, an elaborated analysis on delay, area and power ofdynamic comparators has been presented for numerous architectures.

According to the double-tail structure which is put forward in [9], a very new dynamic comparator was presented, which do not need a high input voltage or stacking of too many transistors as that in the existing literature. Just by adding very few minimum size transistors to the original double-tail comparator structure, the latch delay time was observed to be reduced drastically. Another added advantage to this modification is that a reasonable amount of power is saved when compared to the conventional comparator and double tail comparator.

In this paper, four designs for a comparator are presented. The conventional comparator, double-tail comparator and modified double tail comparator and an enhanced double tail comparator using clock-gating technique. In conclusion a comparison of the performances of all fourdesigns is done and thepower, delay and area are analyzed.

II. CLOCKED REGENERATIVE COMPARATOR

Comparators play a vital role in analog to digital conversion; hence having a high-speed comparator is crucial. Here regenerative comparator provides a helping hand in this case, as these comparators have strong positive feedback. In this paper a brief analysis on power, area and delay is done for the comparator, double tail, modified double tail and proposed design, which uses clock-gating technique to reduce the power consumption.

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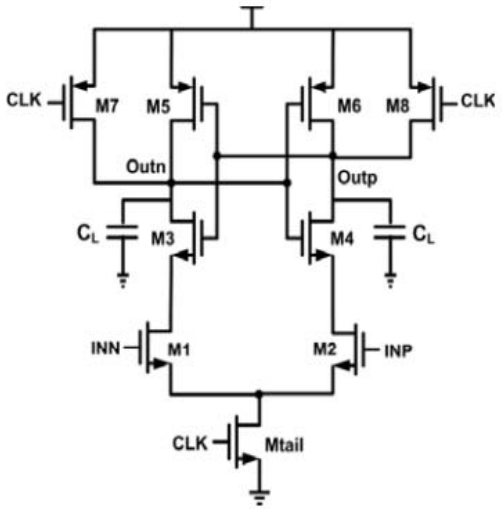

Fig 2. Conventional Comparator

A. *Conventional comparator*

A typical comparator circuit has a TAIL MOSFET and two back to back inverters that operates like a latch..The schematic design for the conventional comparator is shown in Fig 2[1].

The comparator circuit works with the supply voltage of 0.8V and the technology used is 180nm CMOStechnology. Initially when the clk=0 , the TAILMOSFET is OFF soOUTP and OUTN are charged to V_{DD}.When the clock becomes 1, it turns ON the TAIL MOSFET, depending upon the input. If INP>INN, OUTP discharges at much higher rate than OUTN.Once OUTP completely discharges, it turns ON the MOSFET M_5 which pulls back OUTN to V_{DD}.The same process happens when INN>INP.The simulation of the above schematic was performed in CADENCE VIRTUOSO IC 6.1 and their results are shown in Fig 3.

B. *Double tail comparator*

The major difference between a conventional and a double tail comparator is that this circuit is employed with two TAIL MOSFETs thereby providing two paths for the current to discharge. Hence reducing the delay of the circuit. This structure also has less stacking of transistors when compared to the normal comparator. The schematic for the double tail comparator is shown in Fig 4[1].

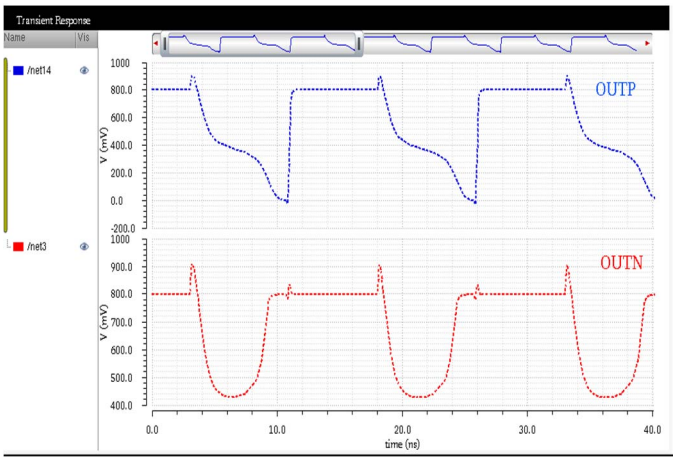

Fig 3. Transient analysis of conventional comparator

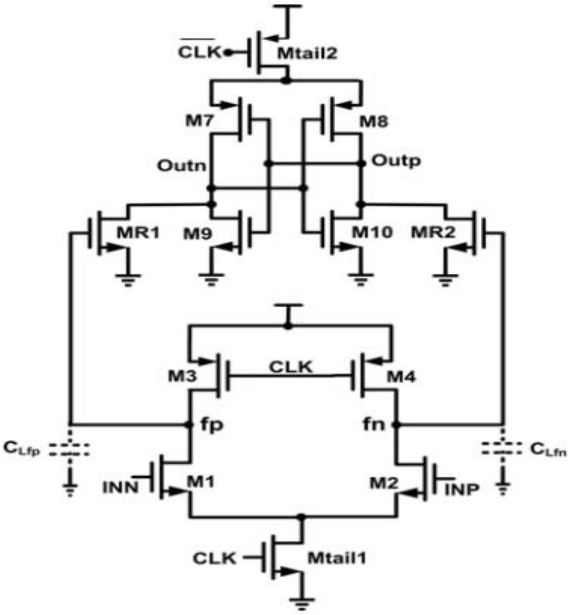

Fig 4. Double-Tail Comparator

During the initial phase (when clock=0), the TAIL1 and TAIL2 MOSFETs are in OFF condition. Due to this,MOSFETS M_3 and M_4 is turned ON which charges $F_N$and $F_P$to V_{DD}. F_N and F_P turn ON the MOSFETs M_{R1} and M_{R2}, which pulls down the node OUTN and OUTP to ground, this turns ON the MOSFETs M_7 and M_8. When clk =1, MOSFETs $M_3$and M_4 are in OFF condition and both the tail MOSFETs are turned ON. OUTN and OUTP are charged to V_{DD} at different rates. If INP > INN,F_N discharges at much higher rate than F_P. During this stage, OUTN gets charged to V_{DD} at a much faster rate than OUTP. As F_N discharges at a higher rate, it turns ON the MOSFET M_{R2} which pulls OUTP back to ground before it can reach V_{DD}. By this time OUTN gets charged to V_{DD}. This can be observed in the simulation results that are obtained from the schematic. The simulation results are shown in Fig 5.

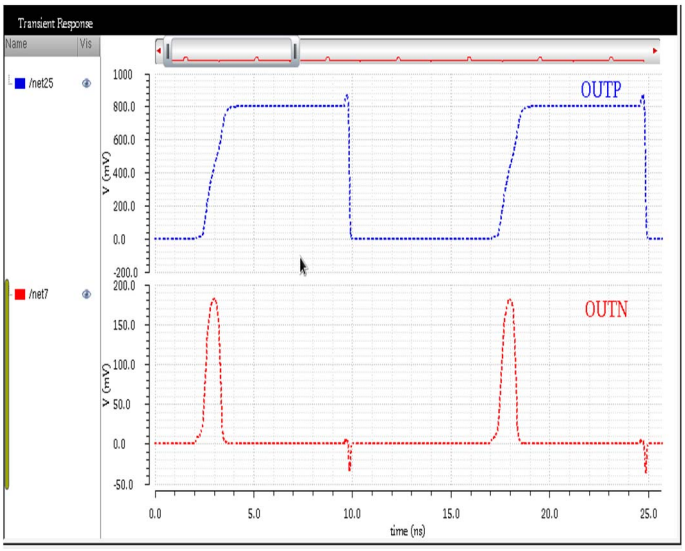

Fig 5. Transient analysis of double-tail comparator

C. Modified double-tail comparator

The schematic of the modified double-tail comparator as is shown in Fig 6[1].When the clk=0, i.e. during the initial phase, its operation is similar to that of a double tail comparator. During the set phase, when clk=V_{DD}, MOSFETs $M_3$and M_4 are in OFF condition thus F_N and $F_P$start to discharge at different rates according to the input voltages. If INP > INN, F_N discharges at a much higher rate than F_P, thereby turning the MOSFET, M_{c1} ON, which pulls F_P back to V_{DD}. By this time M_{c2} is still OFF, thereby allowing $F_N$to discharge completely. When the control transistors either M_{c1}or M_{c2} is turned ON, it leads to the static power consumption in the circuit. To reduce the static power consumption, to the original double tail circuit we introduce the two NMOS (M_{sw1} and $M_{sw2)}$ which act as a switch. The simulation of the above design schematic was done and the simulation results are shown in Fig 7.

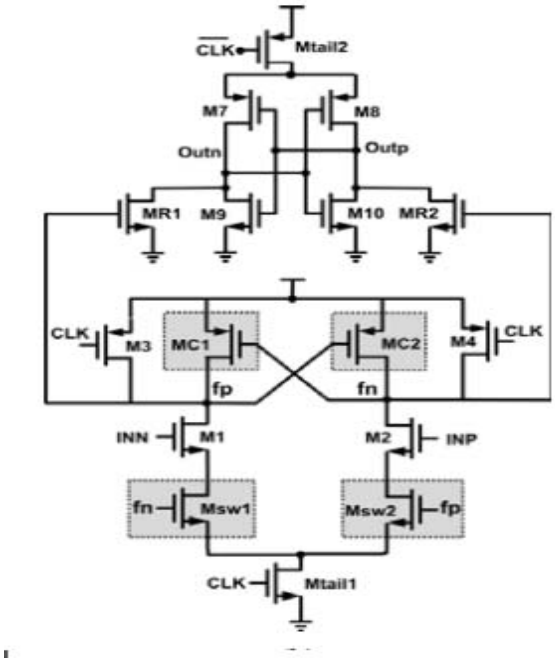

Fig 6. Modified double-tail comparator

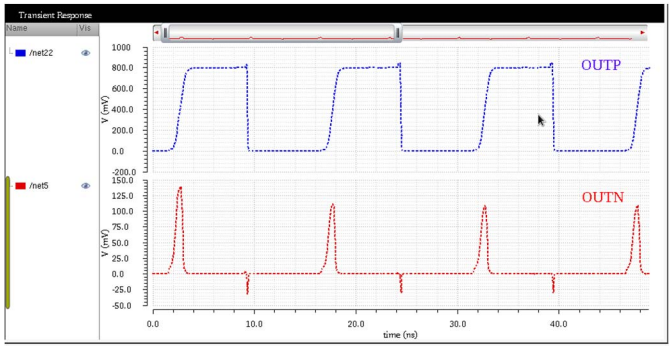

Fig 7. Transient analysis of modified double-tail comparator.

D.Proposed Method using clock-gating technique

In order to further reduce the power consumed by the modified double-tail comparator as proposed in [1], clock-gating technique has been used.

Clock gating is a technique where the clock is kept idle for certain duration of time thereby leading to zero power consumption in the circuit. In this paper, this has been achieved by adding additional logic to the circuit i.e. by compensating on the area, the power of the circuit and the delay is reduced. Here the conventional double tail circuit in [1] has been modified using a NOR gate. A NOR gate is chosen because TAIL2 MOSFET needs to be turned ON only when F_N discharges completely. In other wordsF_N becomes 0. So F_N is given as one of the inputs to the NOR gate and other input is given as pulsating clock signal. Hence when both F_N and clock are zero, the output of NOR gate is high. Hence turning ON the TAIL2 MOSFET. The schematic design of the proposed circuit is as shown in Fig 8.The simulation results for the above design were obtained as shown in the Fig 9.

III.PERFORMANCE ANALYSIS

By performing a detailed analysis on power, area and dealy, the results for the conventional, double tail, modified double tail and proposed comparator have been compared and the results are shown in Table 1.

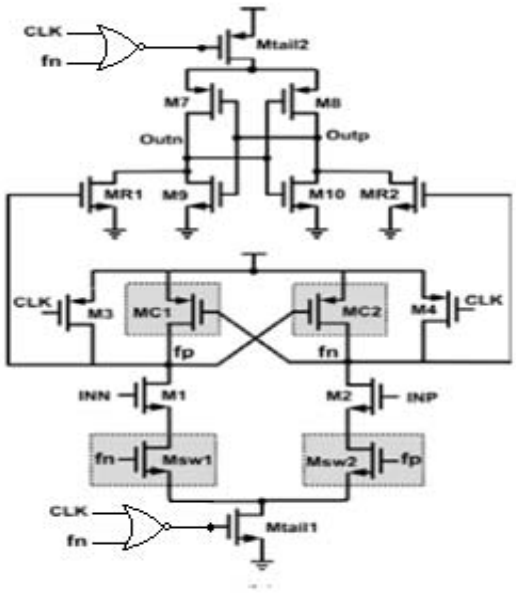

Fig 8. Proposed double-tail comparator with clock gating.

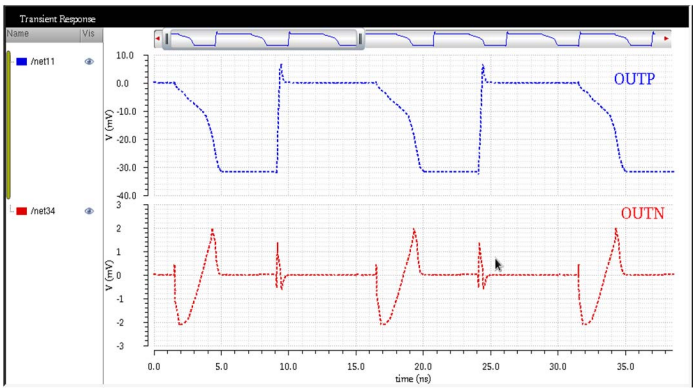

Fig 9. Transient analysis of proposed double-tail comparator.

TABLE I Comparison of the four-comparator designs

Comparator Structure	Conventional	Double-tail	Modified double-tail	Proposed structure
CMOS Technology	180nm	180nm	180nm	180nm
Supply voltage	0.8V	0.8V	0.8V	0.8V
Power consumed	38.54μW	48.05μW	79.54μW	35.5μW
Time delay	41ps	37.9ps	24.5ps	5.1ps
Area occupied	51x51μm	52x49μm	70x68μm	78x80μm

IV. CONCLUSION

In the proposed paper, an elaborate and detailed analysis of four different clocked regenerative comparators, the conventional, Double-Tail, Modified Double-Tail, and proposed comparators were analyzed and simulated. Further these were compared based on Power, Chip area and Delay. The results were obtained from the simulation done using CADENCE VIRTUOSO IC 6.1 software tool in 180 nm CMOS technology. The results show us that the proposed comparator, i.e. modified based on clock-gating technique has shown a very drastic improvement in Power and Delay with a trade-off on the area occupied.

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