Design and Analysis of Double-Tail Dynamic Comparator for Flash ADCs

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***Abstract*—This paper present an analysis of delay and power of the dynamic comparator. As the need for high speed, area efficient and low power analog to digital converters. We are force to go through the dynamic regenerative comparators to maximize speed and power efficiency. A new double tail dynamic comparator is proposed from conventional double-tail comparator for low power and fast operation for low voltage. The new double-tail dynamic comparator reduced delay significantly. At the supply voltage of 1.8V and the sampling frequency of 1.25GHz, the delay and average power of the comparator is 116.2ps and 347.27µW. The proposed dynamic comparator is suitable for flash ADCs. The circuits are simulated with 180nm CMOS- technology in cadence virtuoso. Post-layout analysis of the circuit is done with DRC and LVS check.**

Keywords*— *Double tail Comparator, high speed, low power, Flash ADCs.

I. INTRODUCTION

Comparator is one of the fundamental building blocks of analog to digital convertors. Most of the high speed analog to digital convertors(ADCs) such as flash ADCs, requires high speed and low power comparators with small area. ADC converts an analog signal into digital signal or digitized the signal. For n-bit Flash ADCs 2^n-1 number of comparators is required. Dynamic comparators are used instead of static comparators for fast processing applications [1]. Dynamic comparator is superior to static comparator in light of the fact that they give positive feedback and operate output node faster, and another advantage is, they have low power consumption. Dynamic comparators consist of low gain amplifier integrated with latch circuits. There are two phase in dynamic comparators, in first phase the input of the comparator is compared with reference voltage and the output port is set accordingly at low or high is called evolution phase. During the regeneration phase latch circuit maintains the balance b/w the outputs.

Generally there are two types of comparators current comparator and the voltage comparator. Current comparator consumes less power as compared to the voltage comparator but implementation of the circuit is large and current comparator requires voltage converter circuit as additional circuit. In this paper three different comparators are taken and compared with proposed comparator. The static power dissipation is the disadvantage of the comparator so the power consumption is increased in the comparator. Static power dissipation is reduced in proposed comparator so the static power is negligible so comparator is more efficient and consumes less power and energy. In proposed comparator the output swing is more compared to other comparators. Common mode voltage in proposed comparator is large because of dual rail property; simulation shows variation in delay and avg. power with respect to input voltage and common mode voltage.

In comparator circuit it compares the two input voltages and the digitized output shows which is large. There are two input ports V+ and V- and one digitized output Vo. The equation of Vo is shown-

$$V0 = \begin{cases} 1, \text{if } V_+ > V_- \\ 0, \text{if } V_+ < V_- \end{cases}$$

Now the paper is arranged as follows: in section II describes the type of different conventional comparator with working of comparators followed by pros and cons. proposed comparator is explained in last. Section III contains result and simulation. Simulation shows proposed comparator is fast & used as low power flash ADCs and section IV and V contains layout and conclusion.

II. DYNAMIC COMPARATOR

A. Circuit Implementation And Comparison

The output of the every comparator depends upon the clock input. In this section we discussed about the working of different dynamic circuit. The overall delay of the comparators depends upon the differential pair amplifier delay plus delay of the latch. The conventional dynamic comparator is shown in Figure.1 [2].This is mostly used in ADC with rail to rail output swing with high input impedance and no static power consumption. The working of the conventional comparator is as follows, during reset phase, when clock=0 and M_{tail} is off then transistors M_7 -M_8 is ON and pull the output nodes Out_n and Out_P to V_{DD}. During comparison phase clock =V_{DD} transistor M_7-M_8 are off and M_{tail} is on then output voltage Out_p and Out_n are at pre-charged V_{DD} start discharging at different rate depend upon input voltages. Assume $V_{INP} > V_{INN}$ then Out_p discharge at faster rate. So the PMOS transistor M_5 will turn 'ON' initiative latch regeneration due to back to back inversion. Thus Out_n pull to V_{DD} and Out_p discharges to ground. Drawback of this circuit is that there is only one current path from M_{tail} which is for both latch and differential amplifier. While differential pair require small current for week inversion and obtain long integration interval and better Gm/I ratio. A large tail current is required for fast regeneration in latch.

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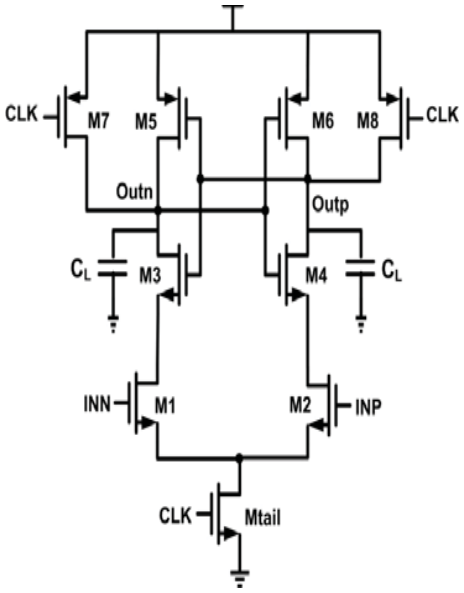

Figure.1: Conventional Dynamic Comparators [2]

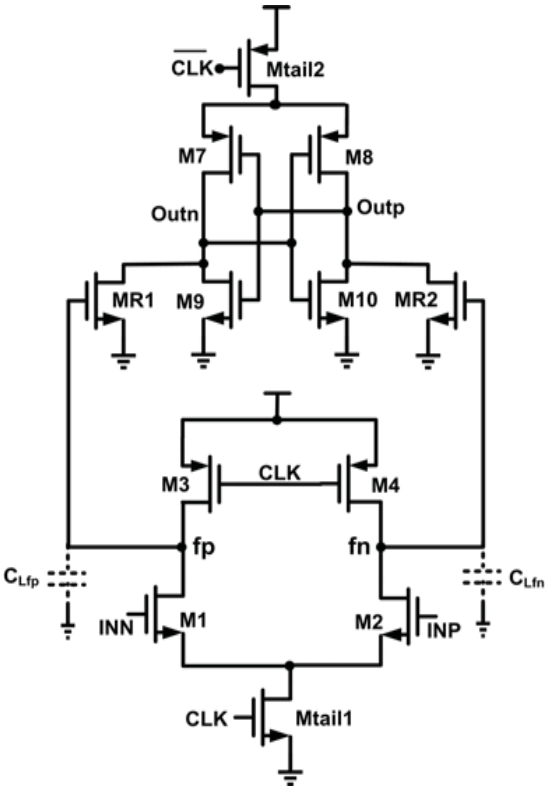

Figure.2: Conventional dynamic comparator [2]

Figure.2 shows the conventional double tail comparator. The double tail enables both a wider M_{tail2} and current in latch state for fast latching independent of small current in input stage and the input common mode voltage (Vcm). Conventional double tail comparator operation is as follows, during rest phase clock=0, $M_{tail1}$and M_{tail2} are OFF, M_3-M_4 are ON and pre-charge the node f_n and f_p to V_{DD} which cause transistor M_{R1}–M_{R2} to turn ON and discharge output nodes to ground. During decision making phase clock=V_{DD}, $M_{tail1}$and $M_{tail2}$is turn ON, so transistor M_3 –$M_4$is turn OFF and node voltage of f_n and f_p starts to drop with different rate depend on $I_{Mtail}/C_{fn(p)}$and the input dependent differential voltage $\Delta V_{fn(p)}$ is build. Intermediate stage M_{R1} and M_{R2} pass $\Delta V_{fn(p)}$ to cross coupled inverters and provide good shielding between input and output transmitter M_9-M_{10} turn ON after the lath regeneration starts. The delay in conventional double tail comparator contains two part t_o and t_{latch}, delay equations are as follows:

$$t_0 = \frac{V_{Thn} C_{Lout}}{I_{B1}} \approx 2\frac{V_{Thn} C_{Lout}}{I_{tail2}}$$

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$

$$t_{delay} = t_0 + t_{latch}$$

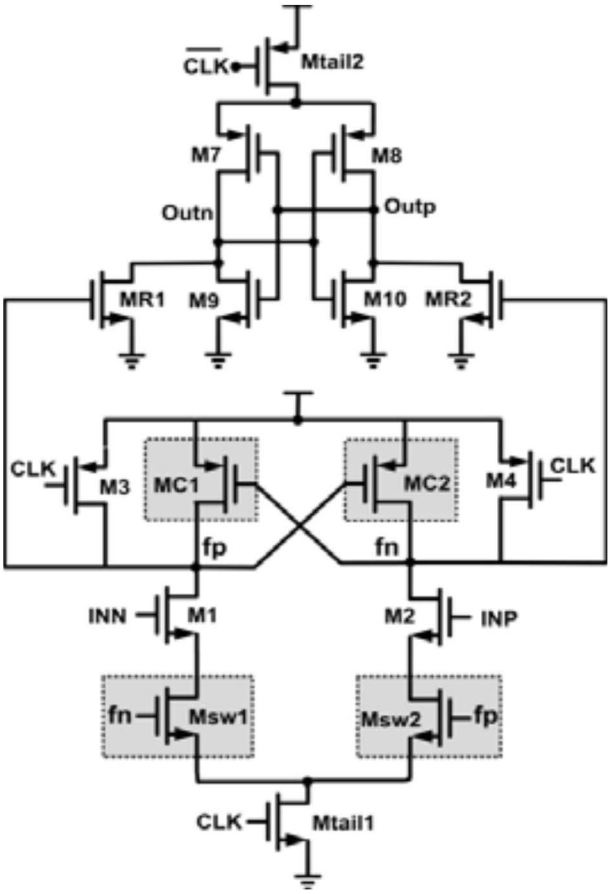

Figure:3 Modified Dynamic Comparator [2]

Figure.3 shows the modified double tail dynamic comparator. In this comparator delay is reduced by increasing latch regeneration speed, in order to do that two controlled transistors are added $M_{c1}$and M_{c2} in parallel with $M_3$and M_4 in cross coupled manner. During the rest phase clock=0, M_{tail1} and M_{tail2} are OFF, transistor M_3– $M_4$are ON and pre-charge node f_n and f_p charge to V_{DD}. Hence M_{c1} –M_{c2}

are cut off, and transmitter M_{R1} and M_{R2} discharge output node to ground. During decision making clock=V_{DD}, M_{tai1} and M_{tail2} are ON , transistor M_3-M_4 are turned OFF and transistor M_{C1}-M_{C2} at beginning remain OFF and node f_n and f_p start drop at different rates depends upon input voltage . Let V_{INP}> V_{INN} then f_n drops faster than f_p at voltage of $M_2$is more, current drown from M_2 is more than M_1.Since f_n is discharge faster comes to ground faster than f_p, so M_{C1} is turn ON first and discharge node f_n to ground, so transistor M_{R1} and M_{R2} are OFF. Since f_n and f_p on dropping but M_{R1} pulls OUT_n to ground faster than OUT_p due to the different charging rate from V_{DD}. In this comparator current from V_{DD} is drown to the ground via tail transistor (M_{C1}, M_1 and M_{tail1}) and input comes in static power consumption too overcome this too NMOS transistor M_{sw1} and M_{sw2} are placed below input transistor as switches. The operation of the controlled transistors with switch enhances the operation of latch.

B. Proposed Comparator

Proposed comparator is modified form of conventional double tail comparator. The proposed comparator is shown in Figure.4. The proposed comparator is faster than the other comparators and also consumes less power. The working of the proposed comparator is same as modified double tail comparator. In this comparator we added two PMOS transistor in latch circuit which provide the better output swing to the circuit and also provide better common mode voltage range.

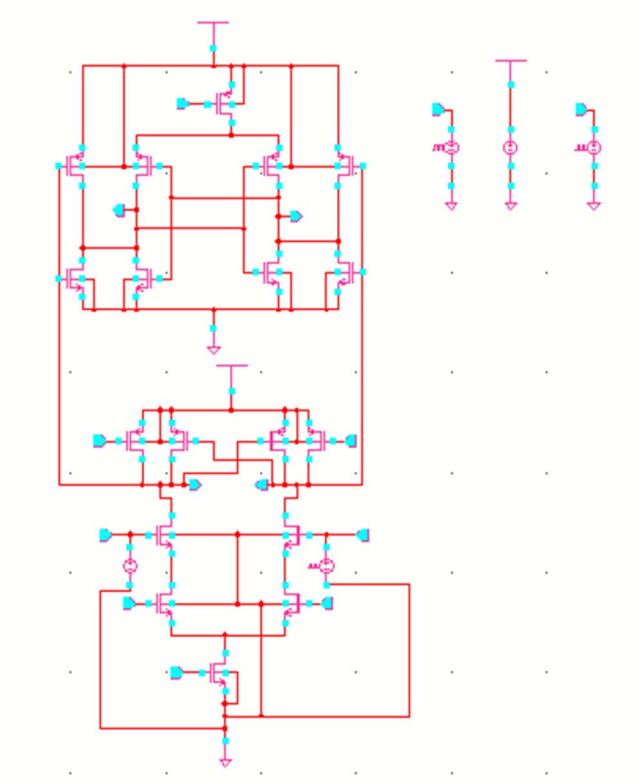

Figure.4: Schematic of a double tail dynamic comparator

At the output node pmos and nmos transistor are presented which provide better amplification. When M_{R1} is 'on' then M_{R2} is 'off' due to the two controlled transistor pair in circuit, thenM_{R4}pull up the output nodes OUT_p to V_{DD} and OUT_n pull down to ground since M_{R3} is 'off'. At the clock frequency of 1.25GHz and ΔVin is 100mV, a delay of 116.2ps is achieved. DC power or static power consumption is 47.448 peco-watt and average power consumption is 347.27µ-Watts. The input common mode range is 0.6 to 1.7V which is grater then the others and provides better output swing and amplification.

TABLE-I PERFORMANCE COMPARISION

Parameters	Conventional Dynamic Comparator	Modified Dynamic Comparator	Proposed Dynamic Comparator
Technology	180nm	180nm	180nm
Supply Voltage	1.8V	1.8V	1.8V
Sampling Frequency	900MHz	2.4GHz	2.5GHz
Delay	181ps	160ps	116ps
Power Consumption	280	338	347
Area	16µ×16µ	28µ×14µ	17µ×25µ
DC Power	NA	0.052n	0.047n

Table I shows the comparison between conventional dynamic comparator, modified dynamic comparators and the proposed dynamic comparator. Proposed comparator consumes least DC or Static power consumption but average power consumption is slightly high that can be negligible. Proposed dynamic comparator have least delay and fast among the others .It is suitable for application in low power and fast operating ADC

III. SIMULATION AND RESULTS

For the comparison of proposed dynamic comparator with conventional dynamic comparator and modified dynamic comparator, all circuit have been simulated in 180nm CMOS technology with the supply voltage of 1.8V. Sampling frequency at 1.25GHz and input frequency at 625MHz with common mode input voltage at 1.7V and ΔVin is 100mV, the output of the proposed comparator is shown in Figure.5 with the delay of 116.2ps and average power of 347.27µW.

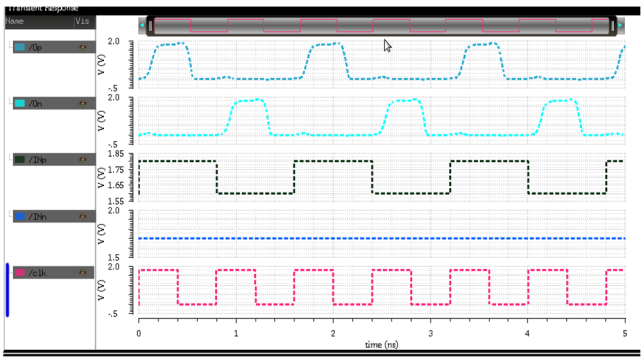

Figure.5: Transient response of proposed dynamic comparator at V_{DD}=1.8V, ΔVin=100mV and Vcm=1.7V

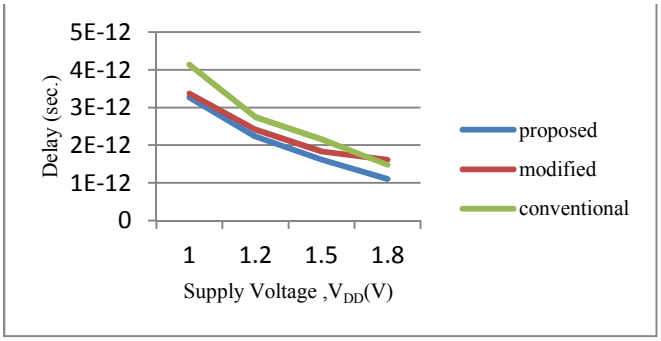

Figure.6: Delay as a function of supply voltage (V_{DD})

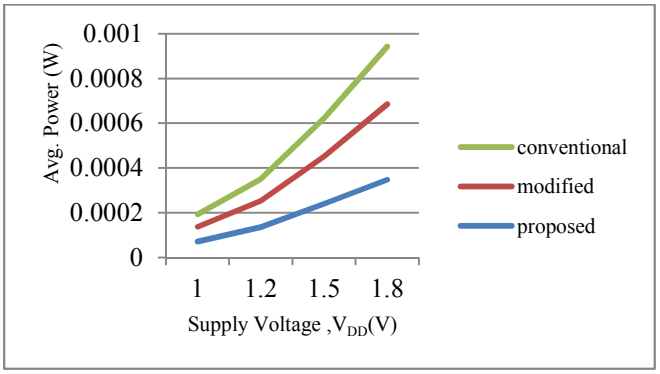

Figure.7: Avg. power as a function of supply voltage

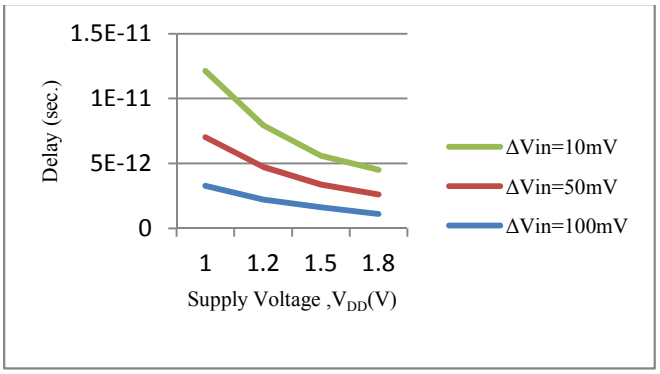

Figure.8: Delay of proposed comparator as a function of supply voltage (V_{DD})

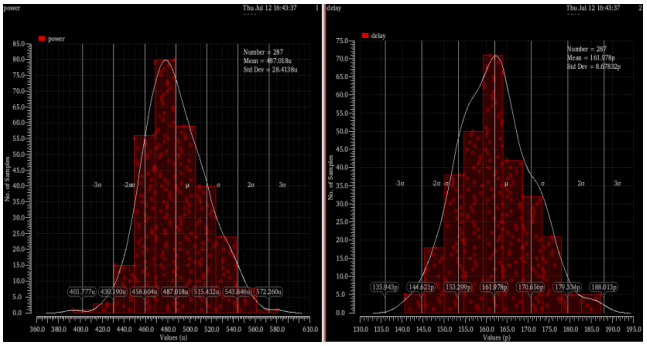

Figure.9: Histogram curve of Monte Carlo analysis.

TABLE II MONTE CARLO ANALYSIS OF COMPARATORS

Comparator	Min.	Max.	Mean	Median	Std. Dev.
Conventional Comparator					
Delay (ps)	125.2	195.8	148.3	146.3	13.03
Avg. Power (µW)	227.4	286.2	258.2	258	11.49
Modified Comparator					
Delay(ps)	134.5	185.3	161.2	160.7	10.5
Avg. Power(µW)	292.6	391.6	338.1	337.9	18.15
Proposed Comparator					
Delay(ps)	116.2	163.3	138.7	139	9.01
Avg. Power (µW)	339.4	470.5	395.9	395.9	23.6

The comparison of the delay is shown in Figure.6 and the comparison of the average power is shown in Figure.7. In order to this simulation variation of change in input voltage ΔVin with respect to supply voltage and delay of proposed comparator is shown in Figure.8. From the analysis and results of the comparators shows that the comparator is reliable and efficient for high speed and low power application. Table II shows the Monte Carlo analysis of the different comparators and Figure.9 shows the histogram of delay and average power of the monte-carlo analysis with σ_{delay}=9.01 and $\sigma_{avg.\ power}$=23.6.

IV. LAYOUT DESIGN

Layout designing started after getting the simulation results as par aspect of proposed LC-DCO. The layout of proposed DCO circuit is shown in figure 6. There are having several rules for layout designing, input and output terminal replace by input output ports and Vdd and ground terminal is replaced by bidirectional port in the schematic of the circuit, than extract the layout in cadence virtuoso layout window. After extract layout arrange the all elements and ports. In cadence virtuoso there having six metals and one poly is available, from these metals and poly designs the layout. Their also available via, which are used as per requirements. Via actually used for one to another wire connection. Via also generate the resistance which is depending on software designing. After layout designing, design rule check (DRC), is to be done using Assura cadence tool. DRC is a verification process in cadence. DRC check design rules, e.g. minimum distance between two metals. After this there some other verifications process is executed that are Layout vs schematic (LVS) check. LVS compare layout to schematic.

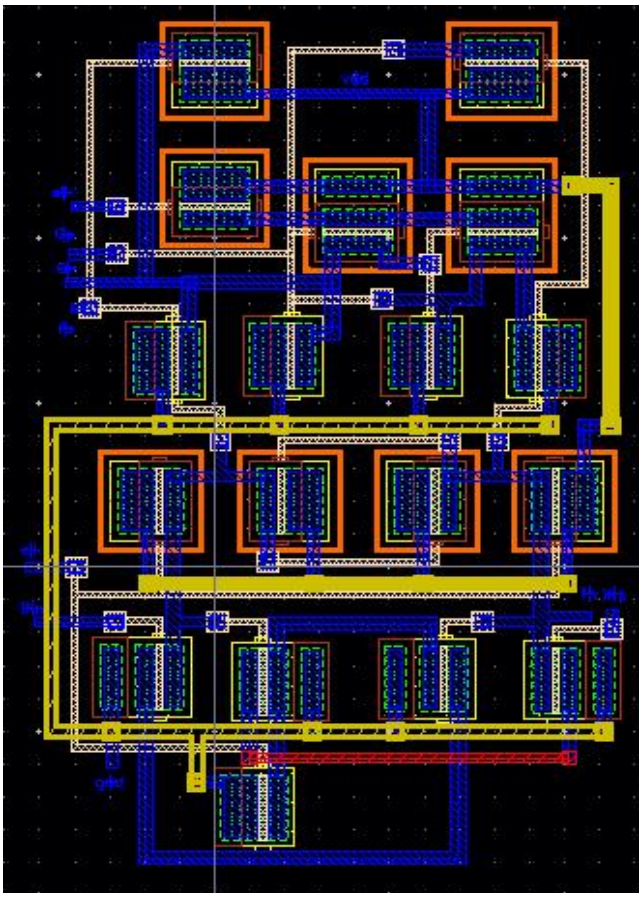

Figure.10: Layout of proposed double tail dynamic comparator

V. CONCLUSION

In this presented paper we analysed the delay for clocked dynamic comparator. In a single tail dynamic comparator there is a single rail which is not sufficient due to large power supply to derive circuit. Single tail dynamic comparator have less output voltage swing, due to the another type of comparator gives rise to double tail comparator provide large output swing and fast operation with low power consumption. Three dynamic comparator are analysed, based on analysis new comparator is proposed to improve the performance. Post layout simulation result in 180nm CMOS technology shows the reduced in delay with greater extant in double tail dynamic comparator.

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