D Flip Flop to SR Flip Flop

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***Abstract*— D Flip Flop to SR Flip Flop is being implemented with 180nm technology and is being presented in this paper. Flip Flop plays a major role in our modern day to day communication system and are efficiently know for its frequency division property. Flip-flops are an integral part of IC systems as they form the core of the timing circuits. Flip Flop are widely uses as counters, shift registers, storage registers, latch , data transfer property and many more.**

Keywords*— *SR Latch, CMOS, Verilog, D Latch

I. REFENCE CIRCUIT DETAILS

D is the actual input of the flip flop and S and R are the external inputs. Eight possible combinations are achieved from the external inputs S, R and Qp. But, since the combination of S=1 and R=1 are invalid, the values of Qp+1 and D are considered as “don’t cares”. The logic diagram showing the conversion from D to SR, and the K-map for D in terms of S, R and Qp are shown below.

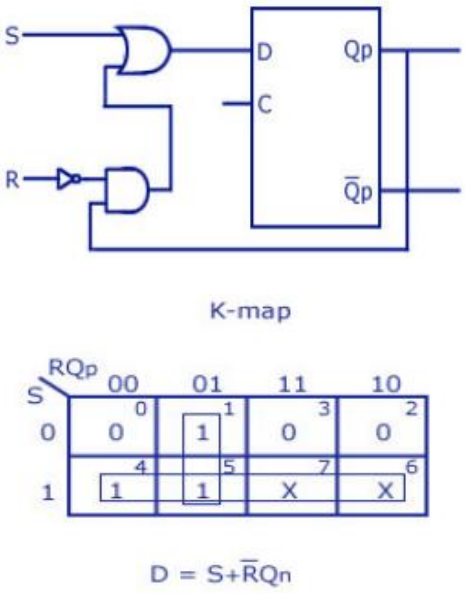

Fig. 1: Block diagram of D Flip Flop to SR Flip Flop

II. REFENCE CIRCUIT DESIGN

A. *Analog Designs Involved*

-D FF

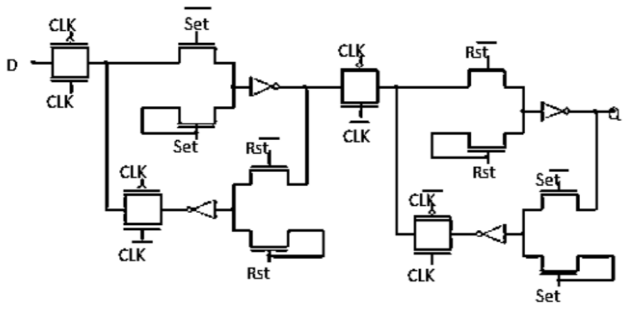

Fig. 1: CMOS implementation of DFF

B. *Digital Implementation Block (VERILOG HDL)*

- *OR Gate*
- *NOT Gate*
- *AND Gate*

III. REFENCE WAVEFORM

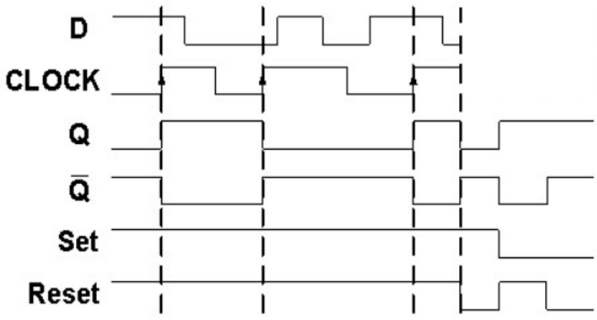

Fig. 4: D Flip Flop to SR Flip Flop

REFERENCES

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