Design and Analysis of Two Input NOR gate in 180nm CMOS Technology

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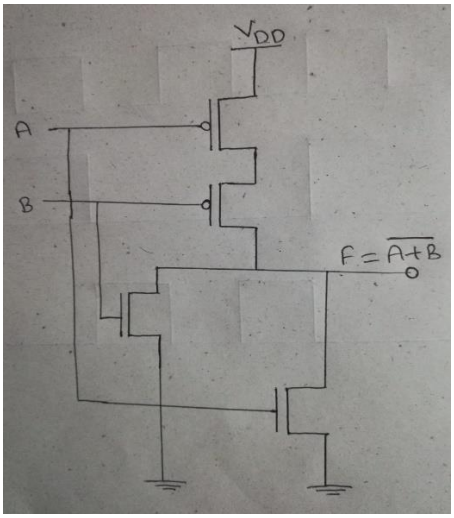
Abstract - The aim of the work is to design a NOR gate in 180nm CMOS technology on esim IC Design platform. In Digital Electronics, a NOR gate is logic circuit which outputs Logic is high when both the inputs are logic low. Other basic gates such as AND, OR, NOT etc. can be designed Using a NOR gate. As it is the series combination of an NOT gate And OR gate. Due to this reason, it is called a UNIVERSAL gate.

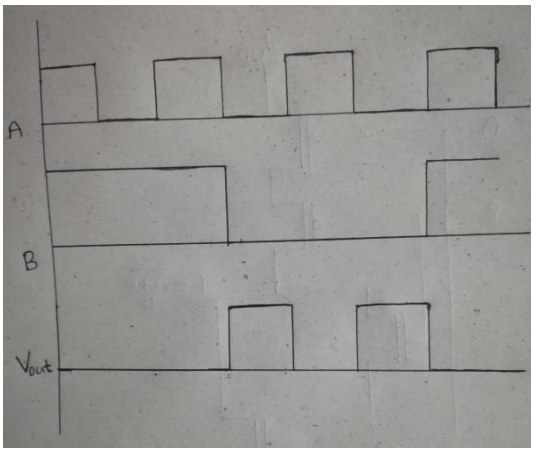
Keywords: NOR Gate, 180nm, CMOS, esim Compiler.

Reference Diagram



Reference Circuit Details - The complementary metal-oxide Semiconductor type NOR gate is designed with the combination Of the PMOS on the top and the NMOS on the bottom. PMOS circuit acts as a pull up network and NMOS circuit acts as a pull down network. For this circuit, the PMOS circuit is connected in series and NMOS circuit is connected in parallel. If two inputs are logic 0, then the output will be high. If one of the inputs is logic 0, then the output will be low. If two inputs are Logic 1, then the output would be low.

Waveforms



Reference: https://www.ques10.com/p/26345/draw-2-input-cmos-nor-gate-and-using-equivalent--1/?