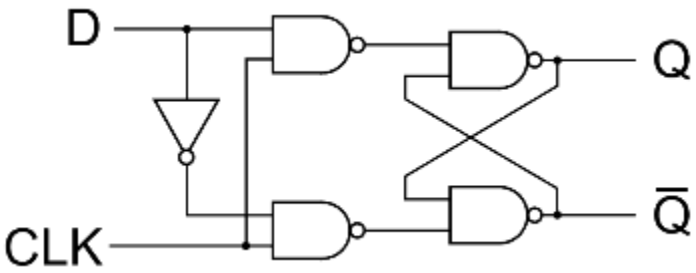
Experiment 7

Aim: To verify the truth table of D flip Flop

Theory:

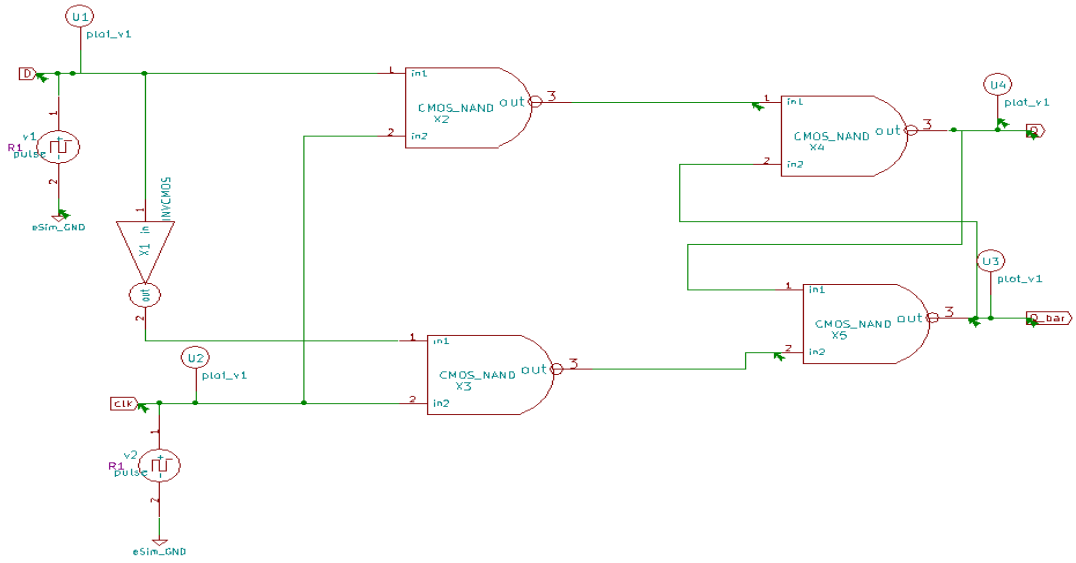
D flip-flop is a better alternative that is very popular with digital electronics. They are commonly used for counters and shift-registers and input synchronization. In this, the output can be only changed at the clock edge, and if the input changes at other times, the output will be unaffected.

Circuit Diagram:

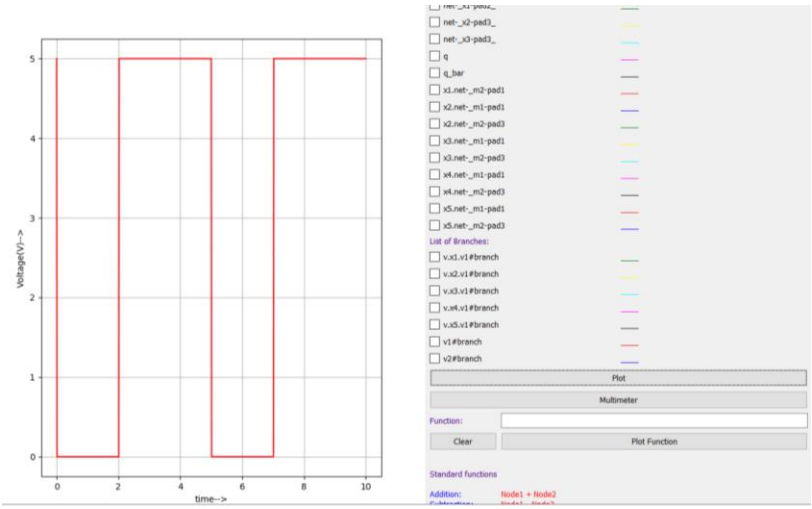


Clock	D	Q	Q’
↓ » 0	0	0	1
↑ » 1	0	0	1
↓ » 0	1	0	1
↑ » 1	1	1	0

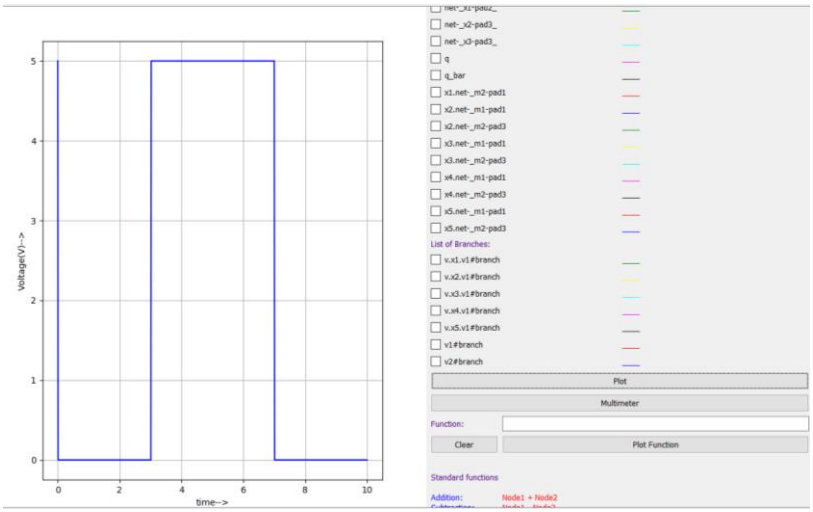
Circuit Diagram:



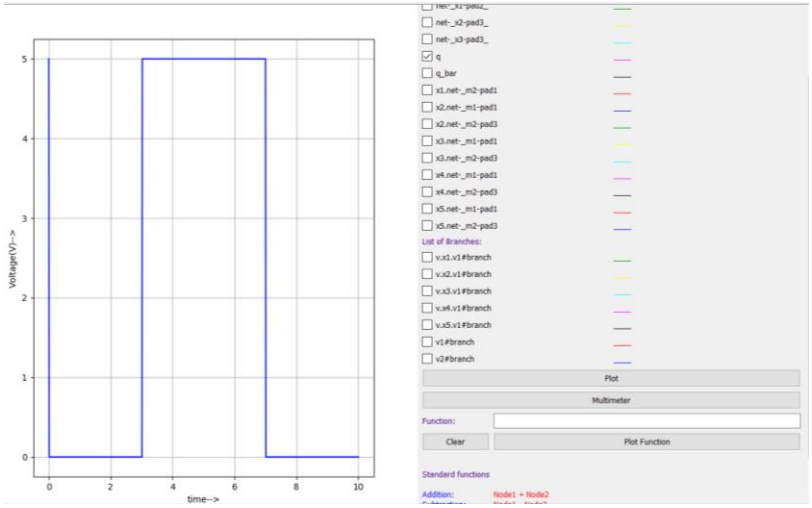
Python plot input D:



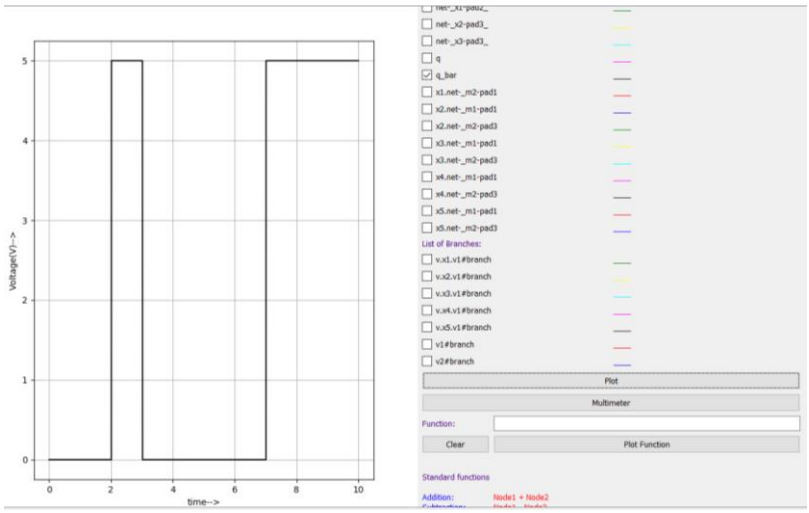
Python plot input clk:



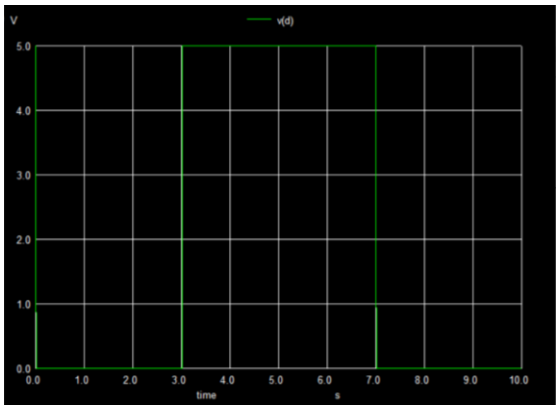
Python plot output Q:



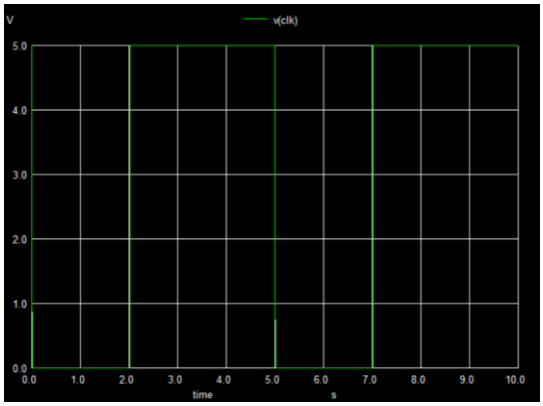
Python plot input Q_bar:



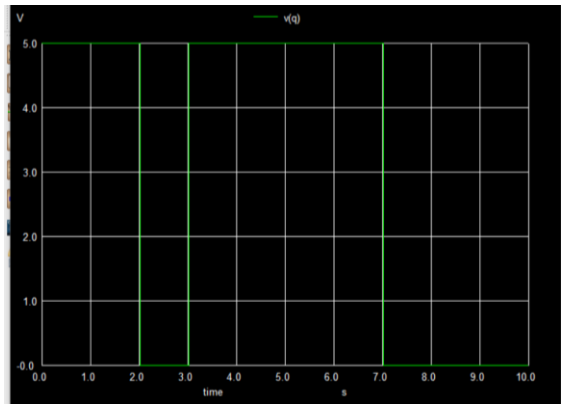
NGSPICE plot of input D:



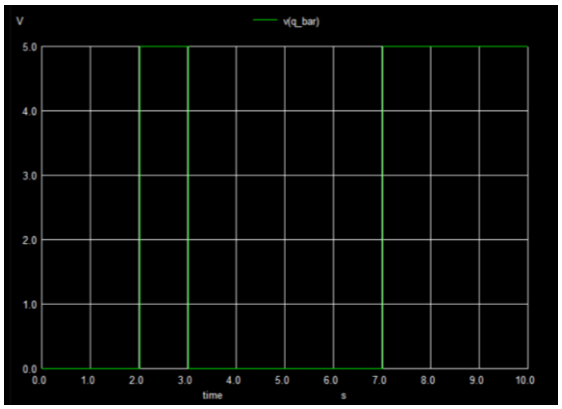
NGSPICE plot of input clk:



NGSPICE plot of q:



NGSPICE plot of Q_bar:



Source/Reference(s) :

1)CMOS VLSI Design A circuit and systems perspective by Neil H.E.Weste,David M.Harris. fourth edition.\

2) Digital logic and computer Design by Morris Mano

3) https://www.electronicsforu.com/technology-trends/learn-electronics/flip-flop-rs-jk-t-d