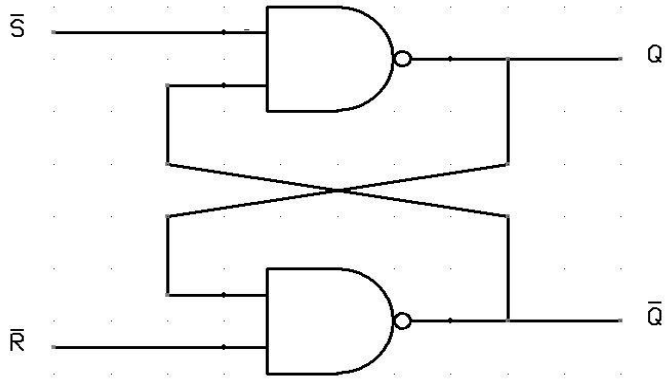
Experiment 8

Aim: To Verify truth table of SR Latch

Theory:

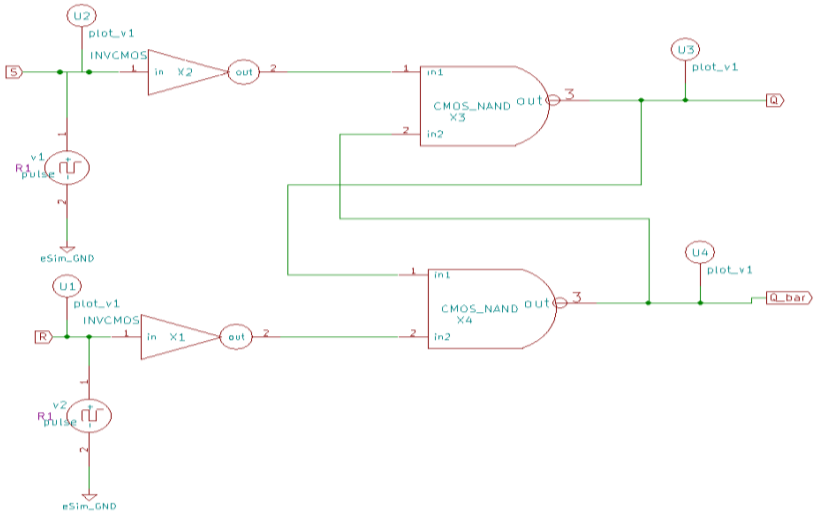
In this circuit when Set S as active the output Q would be high and Q' will be Low. This is irrespective of anything else. (This is an active-low circuit so active here means low, but for an active high circuit active would mean high)

Circuit Diagram:

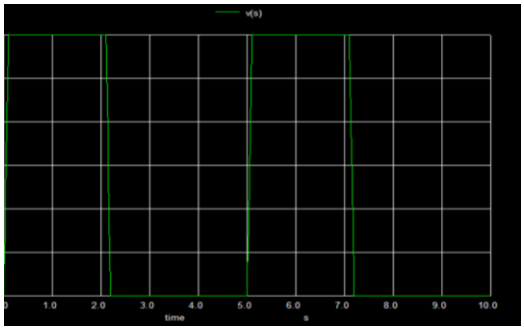


S	R	Q	Q'
0	0	0	1
0	1	0	1
1	0	1	0

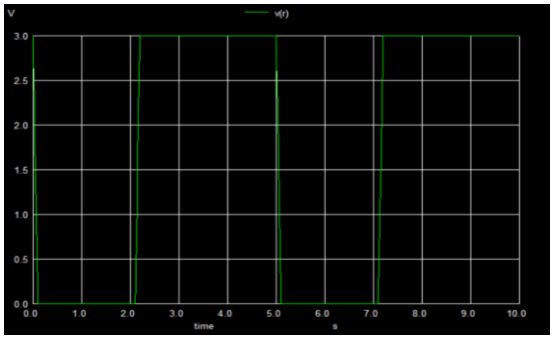
Circuit diagram:



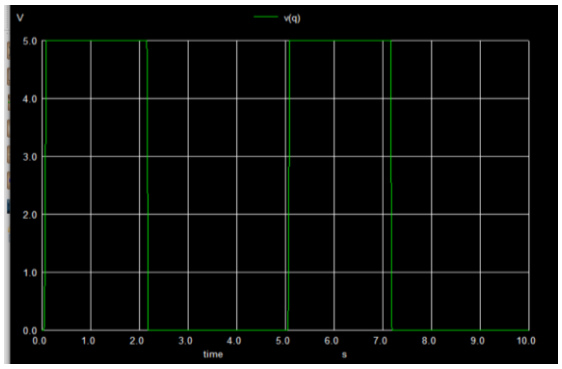
NGSPICE Plot of input s:



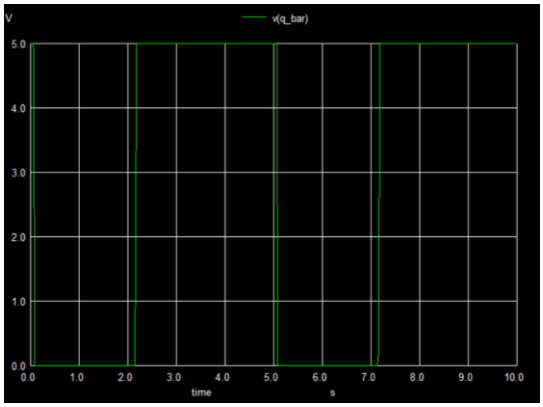
NGSPICE Plot of input R:



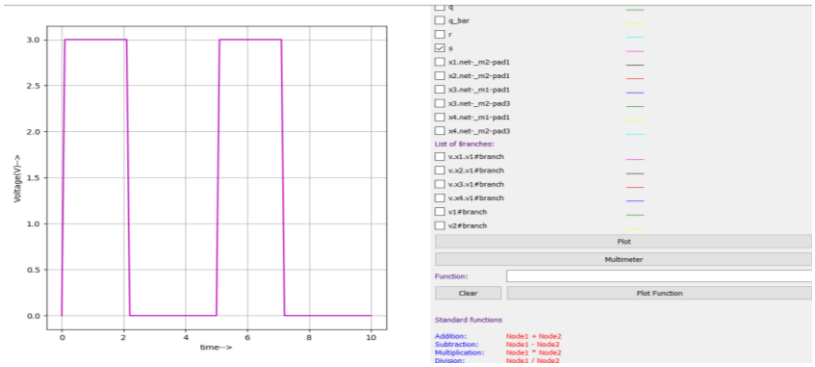
NGSPICE plot of q:



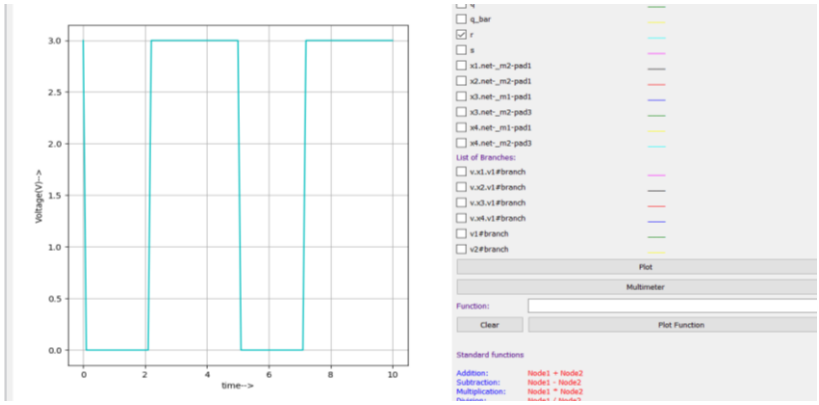
NGSPICE plot of q_bar:



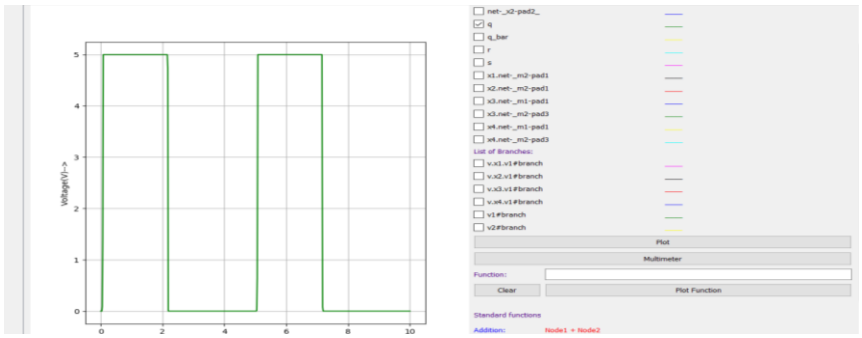
Python Plot of input s:



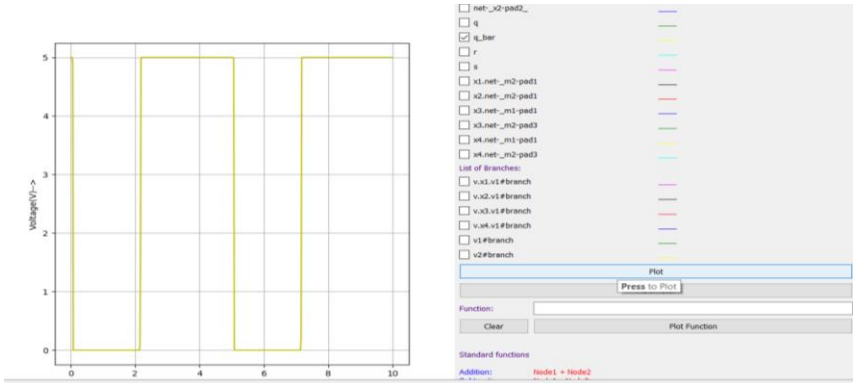
Python Plot of input r:



Python Plot of output q:



Python Plot of output q_bar:



Source/Reference(s) :

1)CMOS VLSI Design A circuit and systems perspective by Neil H.E.Weste,David M.Harris. fourth edition.\

2) Digital logic and computer Design by Morris Mano

3) https://www.electronicsforu.com/technology-trends/learn-electronics/flip-flop-rs-jk-t-d