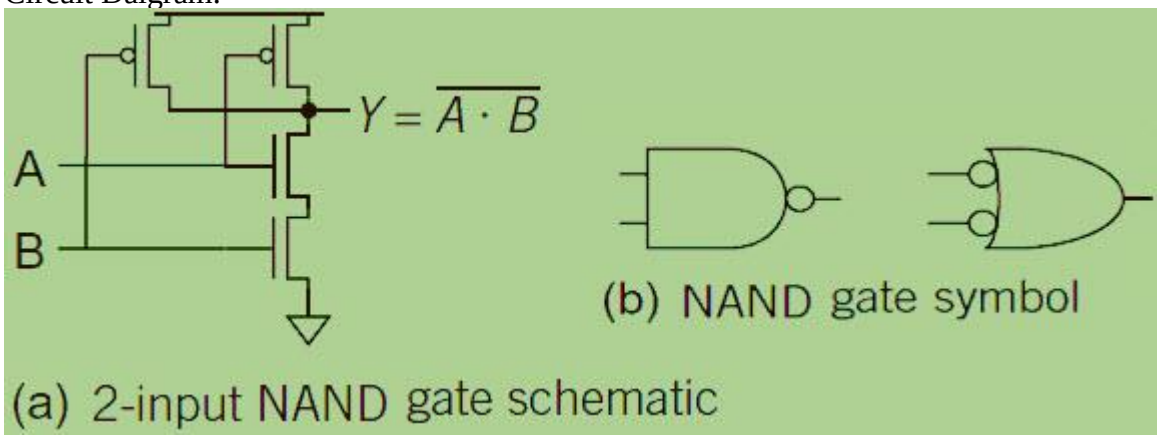
Experiment No: 02

Problem statement: Simulate Schematic of CMOS two input NAND gate and do ERC and transient analysis.

Circuit Daigram:



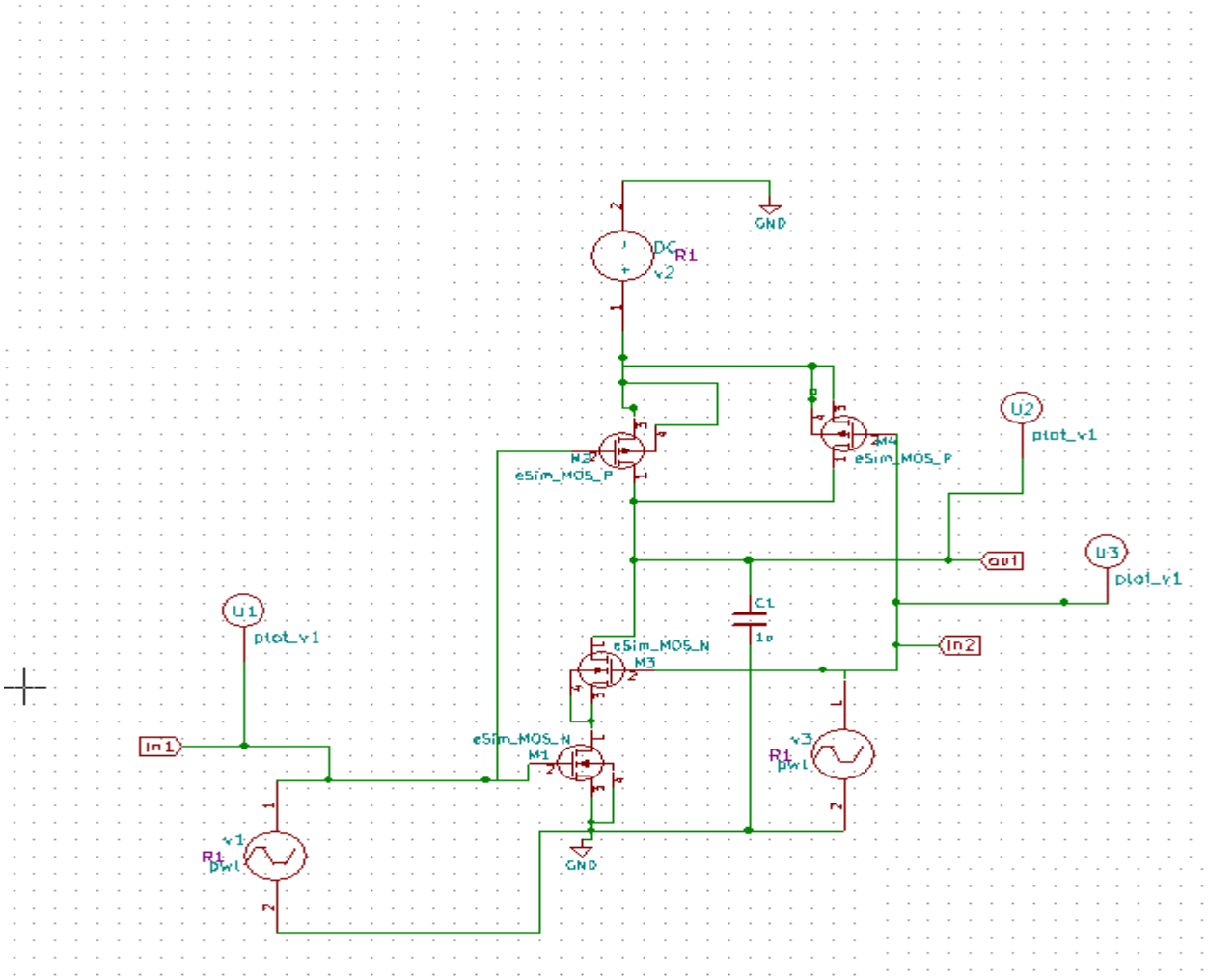
Theory:

The below figure shows a 2-input Complementary MOS NAND gate. It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and VDD.

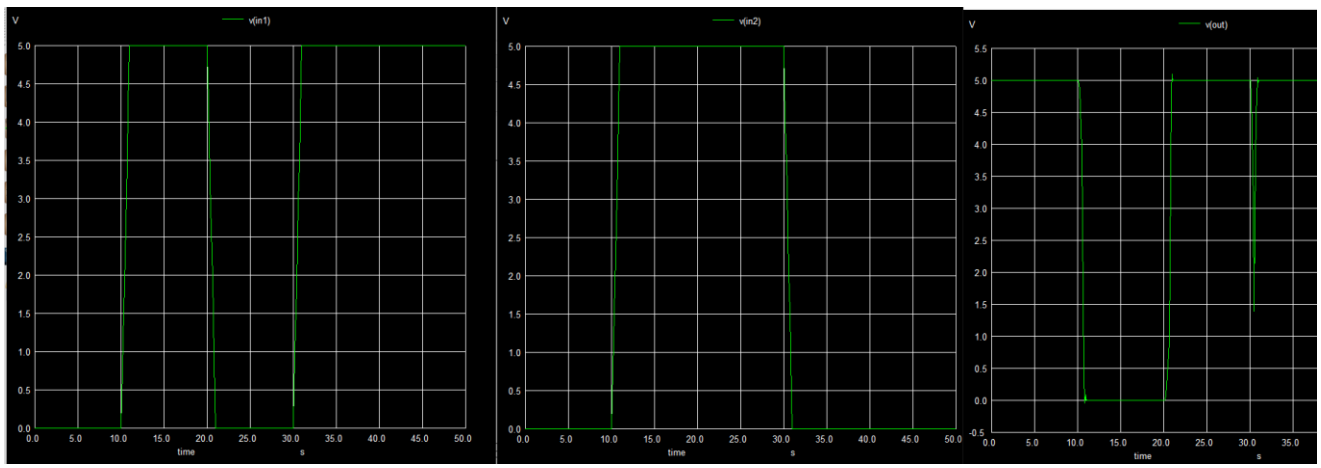
If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.

Hence, the output Y will be high. If both inputs are high, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be logic low. The truth table of NAND logic gate given in below table.

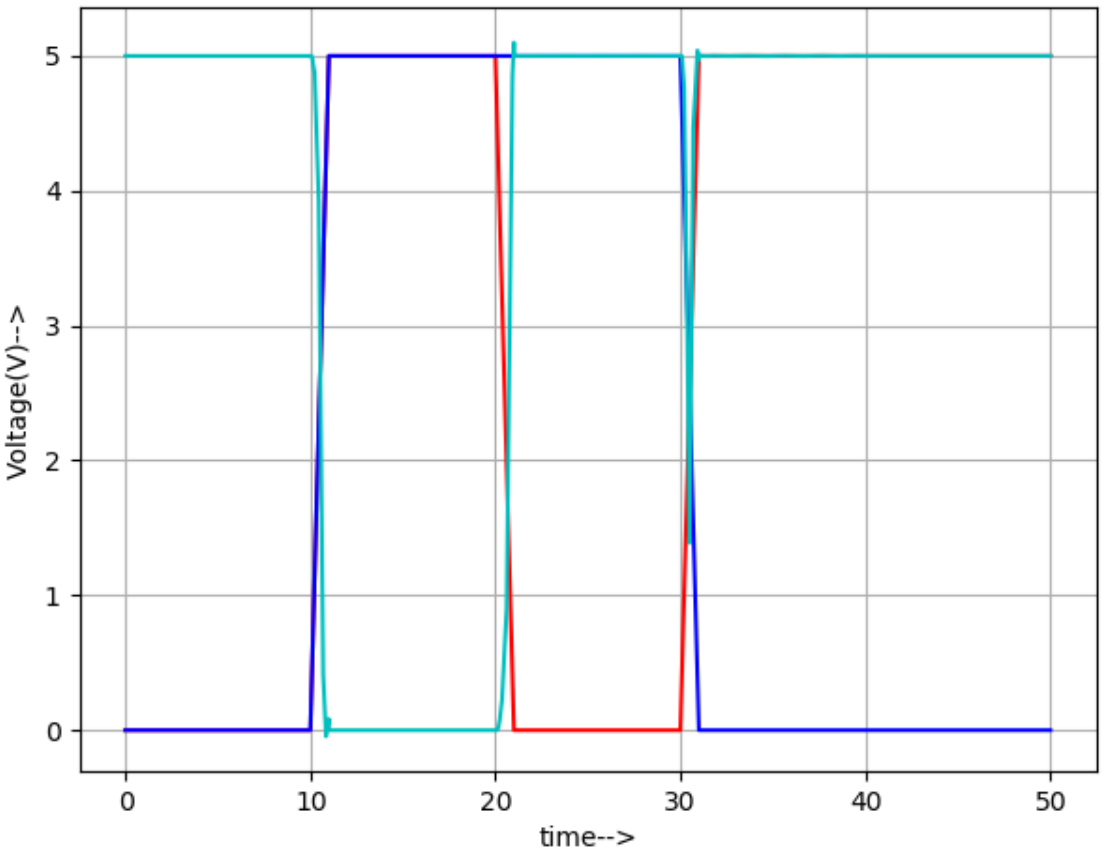
A	**B**	**Pull-Down Network**	**Pull-up Network**	**OUTPUT Y**
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0



Schematic of CMOS NAND



Result in ngspice window



Result in Python Window

Conclusion: Hence we studied could make the schematic and test the working of CMOS NAND gate with two input and it is showing correct results.

Reference:https://www.elprocus.com/cmos-working-principle-and-applications/