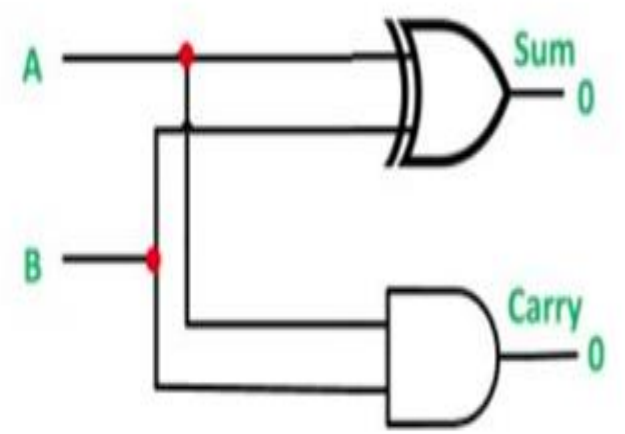
Experiment No: 07

Problem Statement: Simulate Schematic of CMOS Half adder and do ERC and transient analysis.

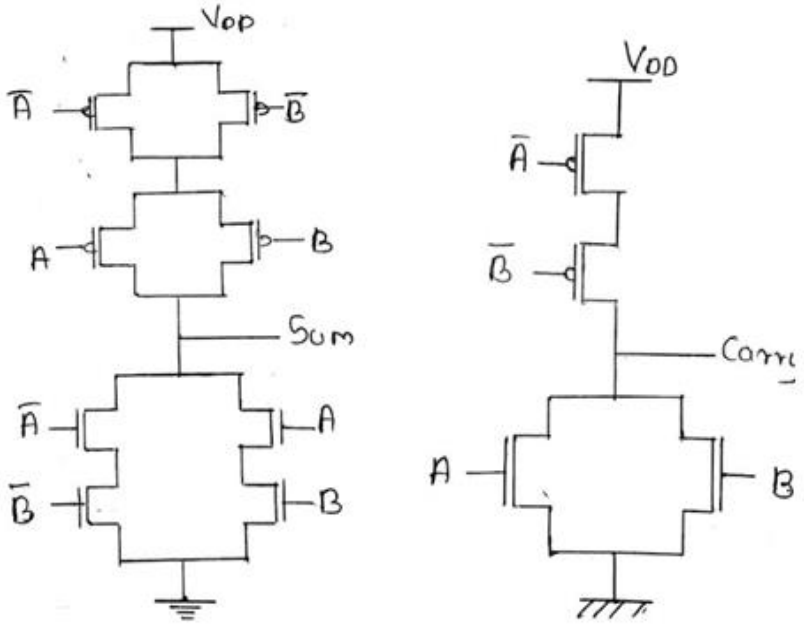
Theory:

Half adder gives two output. First is sum and second is carry. The sum is generated through xor operation and carry is generated through and operation.

A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Logic Diagram and Truth table of Half Adder



Circuit Diagram of CMOS Half Adder

Truth table of Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

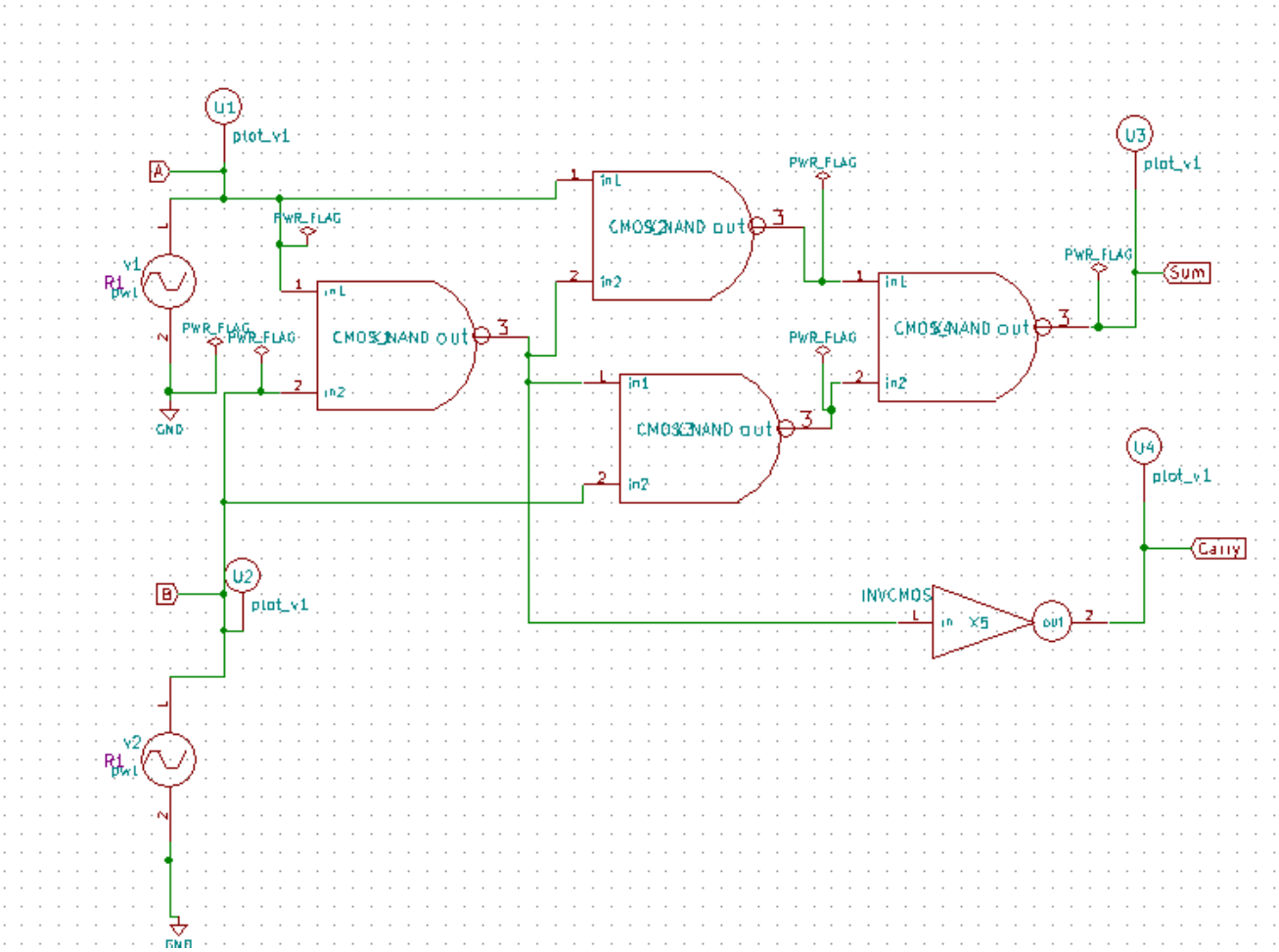
Half Adder Equation

$$S=A'B+AB'$$

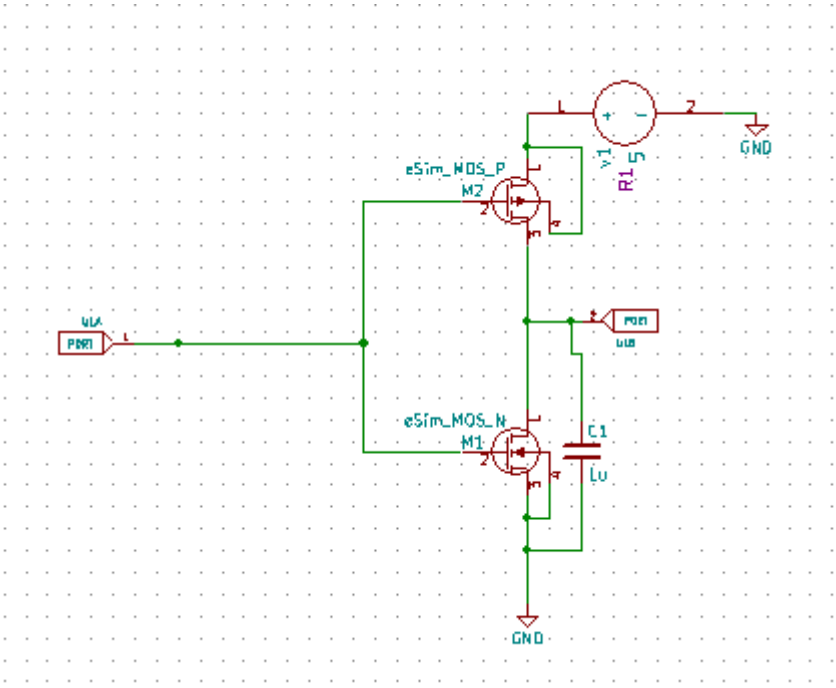
$$C=AB$$

The ALU (arithmetic Logic Unit) of a computer uses half adder to compute the binary addition operation on two bits.

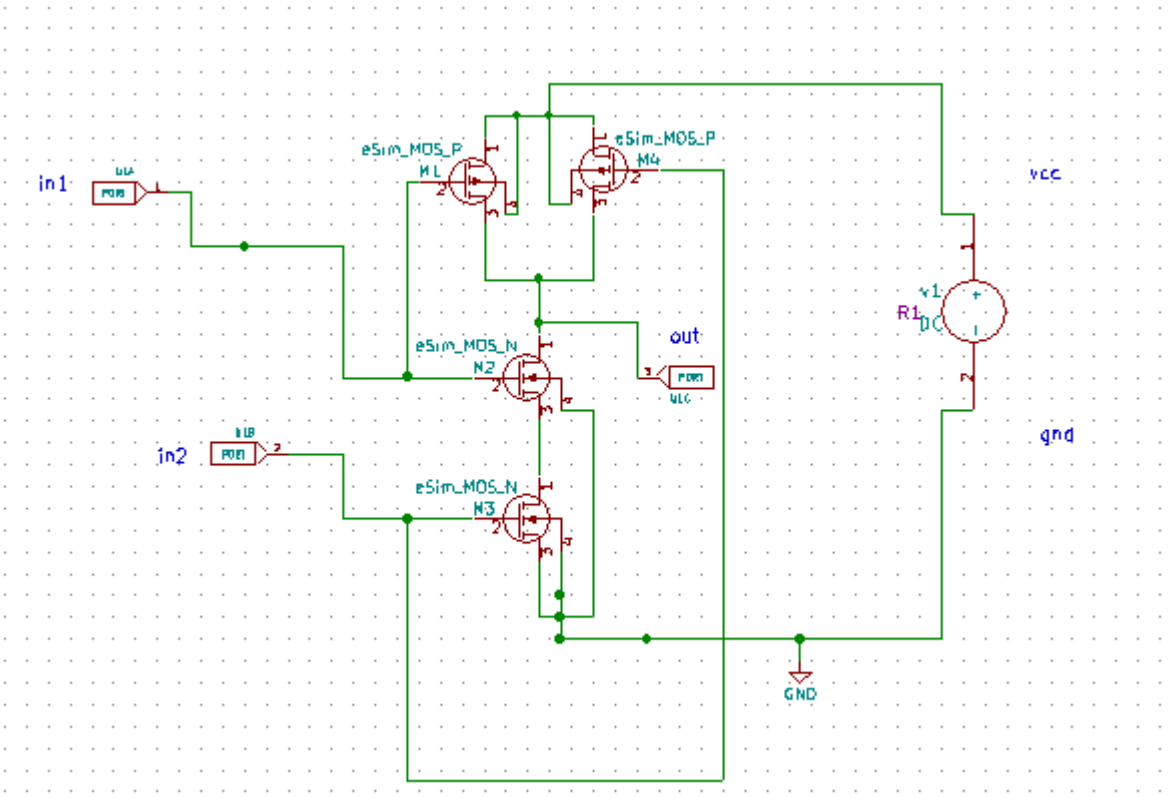
Half adder is used to make full adder as a full adder requires 3 inputs, the third input being an input carry i.e. we will be able to cascade the carry bit from one adder to the other.



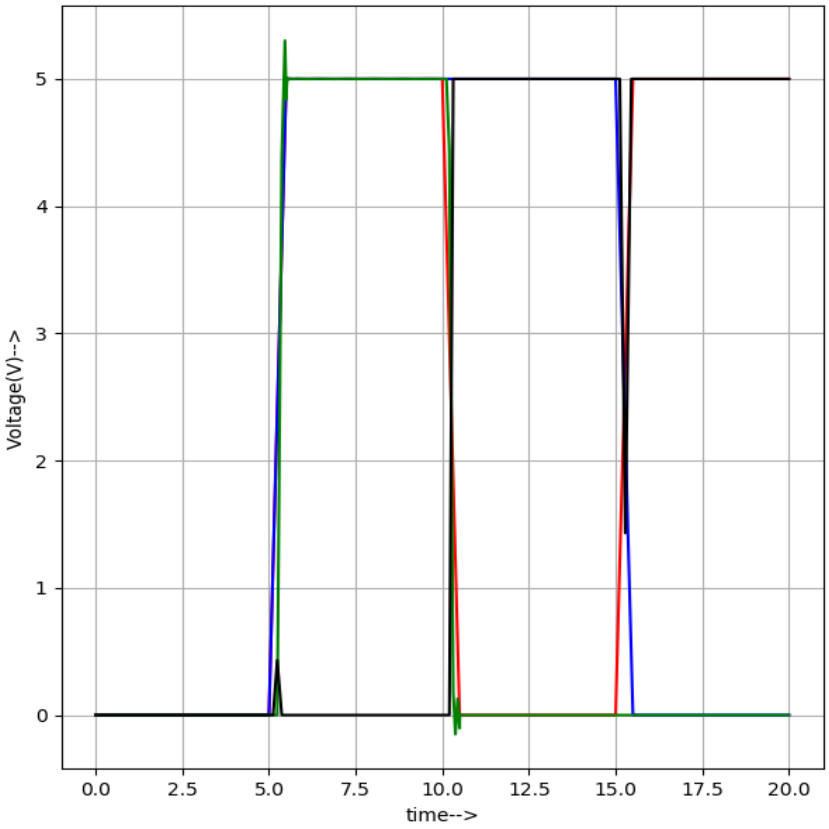
Schematic of Half adder using sub-circuit NAND and Inverter



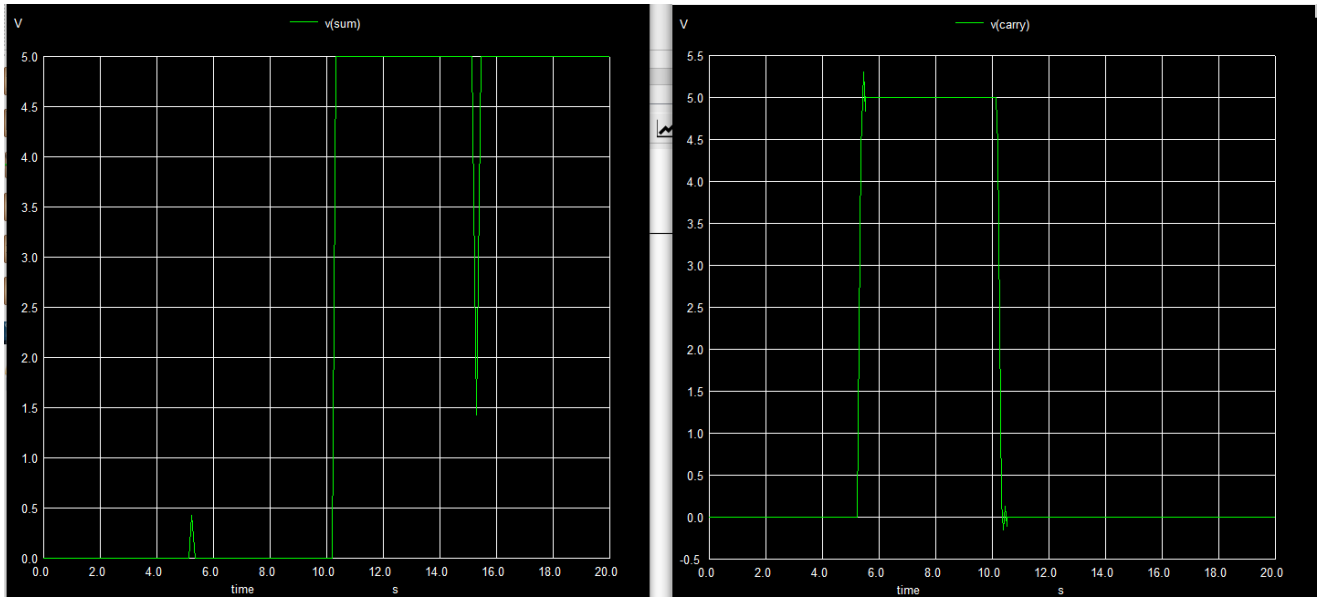
Schematic of sub-circuit inverter



Schematic of sub-circuit NAND



Result output in python window



Result output in Ngspice window

Conclusion: Hence we studied could make the schematic and test the working of CMOS

halfadder and it is showing correct results.
Reference: https://www.ques10.com/p/36440/implement-half-adder-circuit-using-static-cmos/