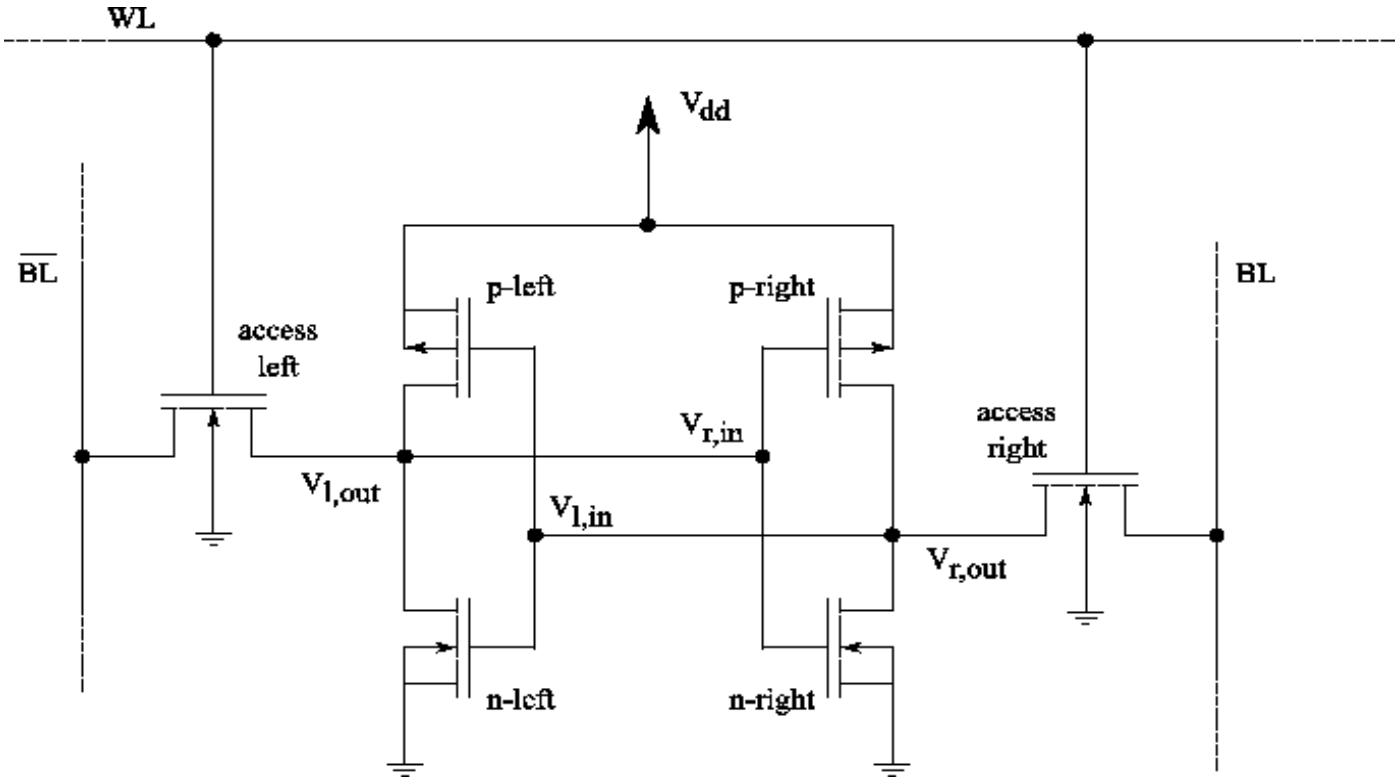
Experiment No: 10

Problem Statement: Simulate Schematic of CMOS 6T SRAM and do ERC and transient analysis. Name of the experiment: CMOS Inverter

Circuit diagram:



Theory:

6T SRAM Cell is a Circuit of a 6 transistor SRAM cell. It consists of two CMOS inverters and two access MOSFETs.

Static random access memory (SRAM) can retain its stored information as long as power is supplied. This is in contrast to dynamic RAM (DRAM) where periodic refreshes are necessary or non-volatile memory where no power needs to be supplied for data retention, as for example flash memory. The term ``random access'' means that in an array of SRAM cells each cell can be read or written in any order, no matter which cell was last accessed.

The core of the cell is formed by two CMOS inverters, where the output potential of each inverter Vout is fed as input into the other Vin. This feedback loop stabilizes the inverters to their respective state.

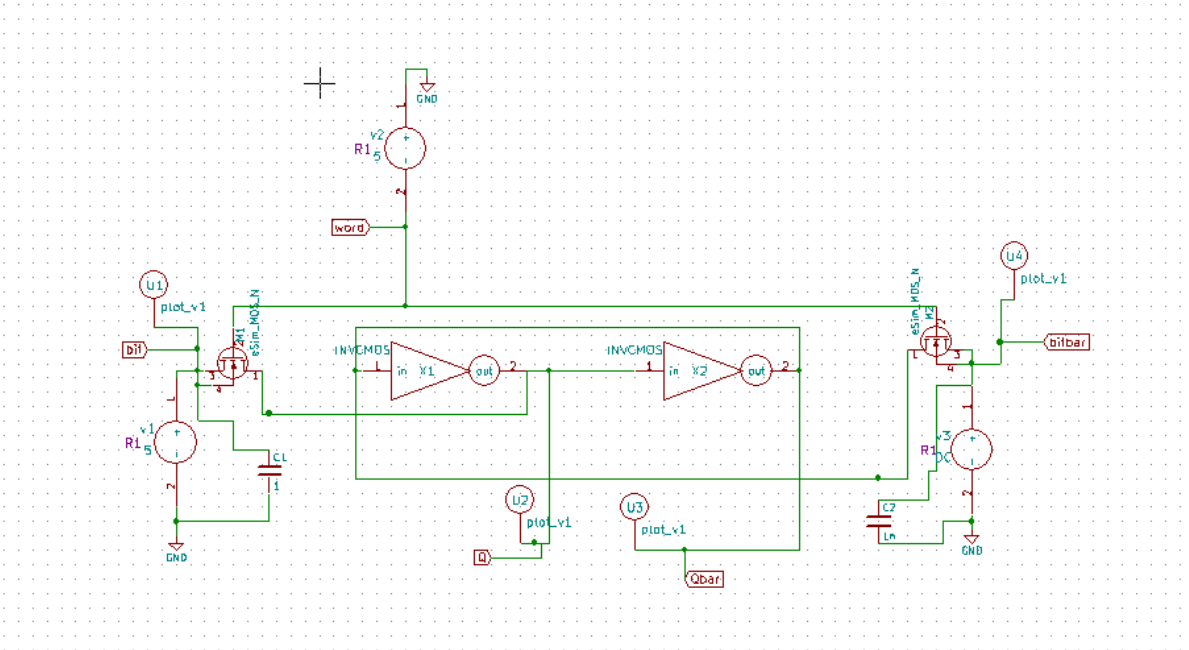
The access transistors and the word and bit lines, WL and BL, are used to read and write from or to the cell. In standby mode the word line is low, turning the access transistors off. In this state the inverters are in complementary state. When the p-channel MOSFET of the left inverter is turned on, the potential VL,out is high and the p-channel MOSFET of inverter two is turned off, Vr,out is low.

To write information the data is imposed on the bit line and the inverse data on the inverse bit line, $\overline{BL}$. Then the access transistors are turned on by setting the word line to high. As the driver of the bit lines is much stronger it can assert the inverter transistors. As soon as the information is stored in the inverters, the access transistors can be turned off and the information in the inverter is preserved.

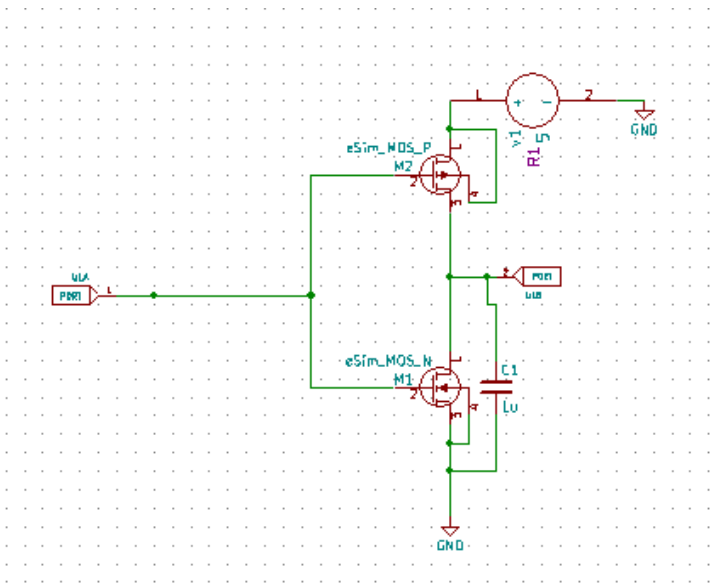
For reading the word line is turned on to activate the access transistors while the information is sensed at the bit lines.

DIN	nWE	wordline	Bitline	data+ (new data)
*	1	0	Z	data (cell passive, stores)
*	1	1	data	data (read cell)
0	0	0	0	data (cell passive, stores)
1	0	0	1	data (cell passive, stores)
0	0	1	0	0 (write 0)
1	0	1	1	1 (write 1)

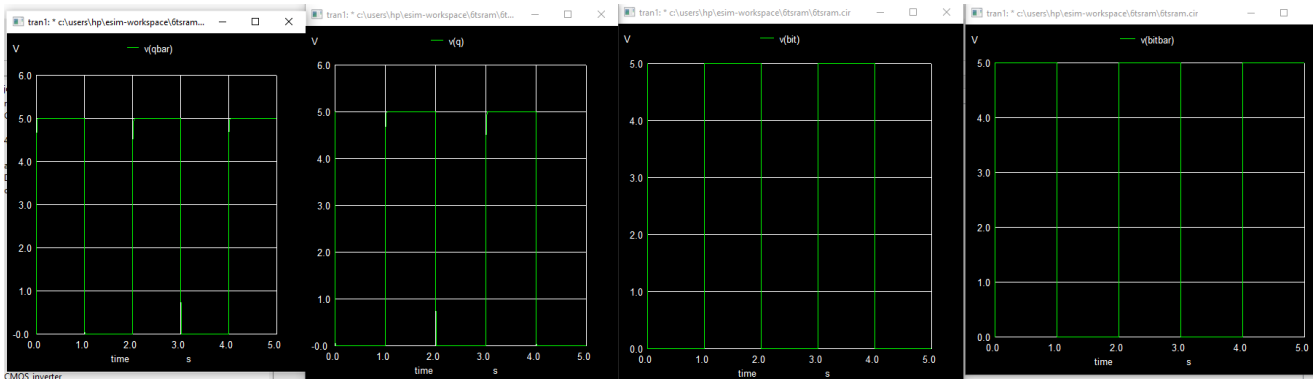
It uses six transistors to store and access one bit.



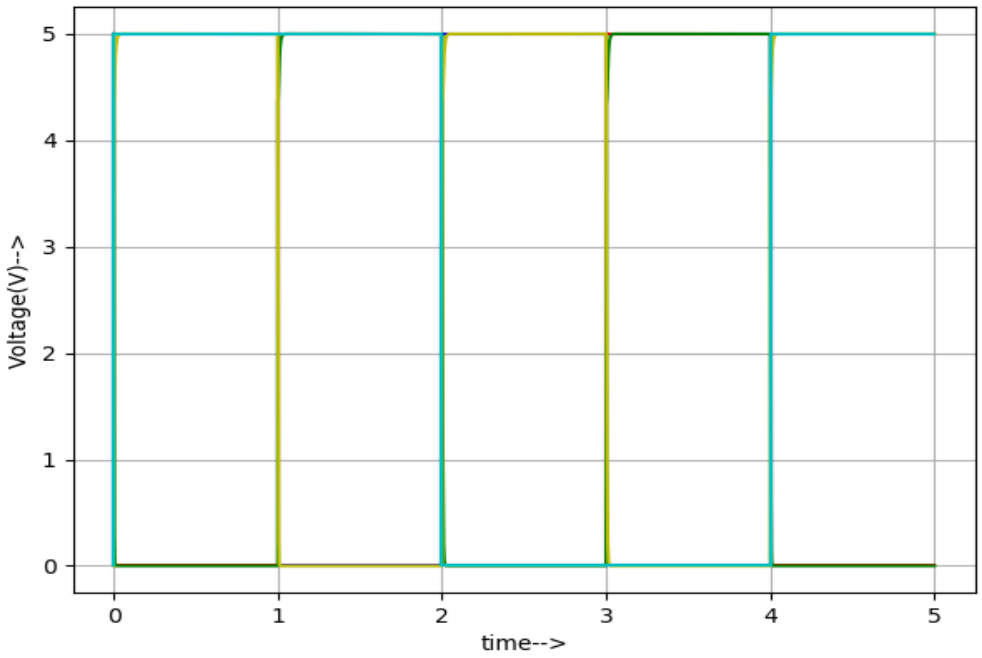
Schematic of 6TSRAM using inverter subcircuits



Schematic of inverter subcircuits



Result in ngspice window



Result in python window

Conclusion: Hence we studied could make the schematic and test the working of CMOS 6T SRAM and it is showing correct results.

Reference: https://www.iue.tuwien.ac.at/phd/entner/node34.html