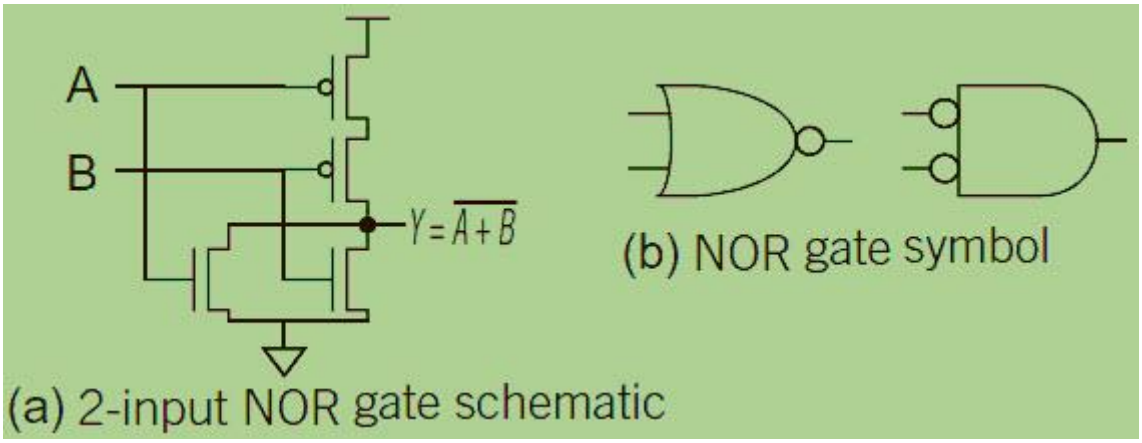
**Experiment No: 03**

Problem Statement: Simulate Schematic of CMOS two input NOR gate and do ERC and transient analysis.

Circuit daigram:



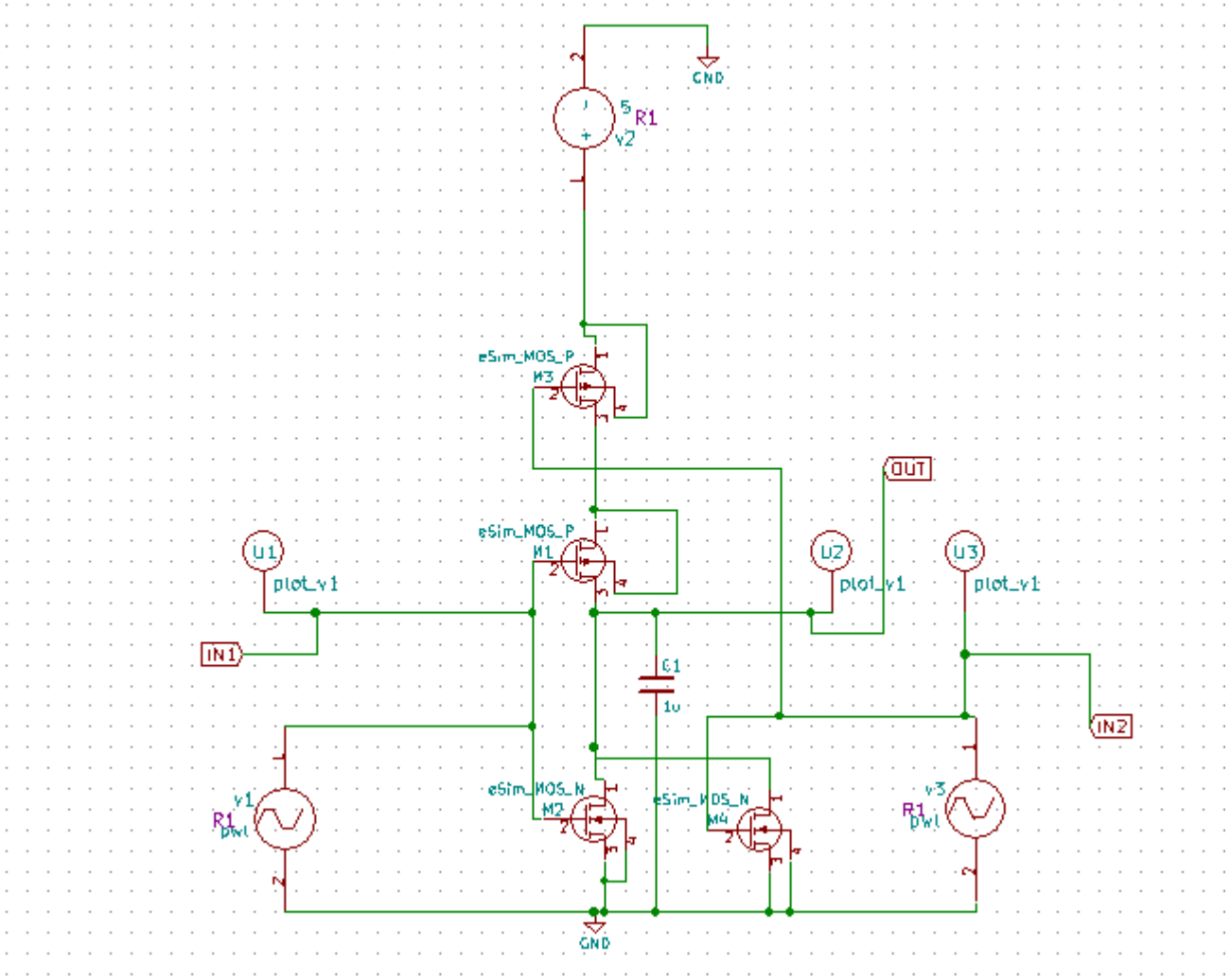

Complementary MOS NOR Gate

Theory: A 2-input NOR gate is shown in the figure above. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in below table. The output is never left floating.

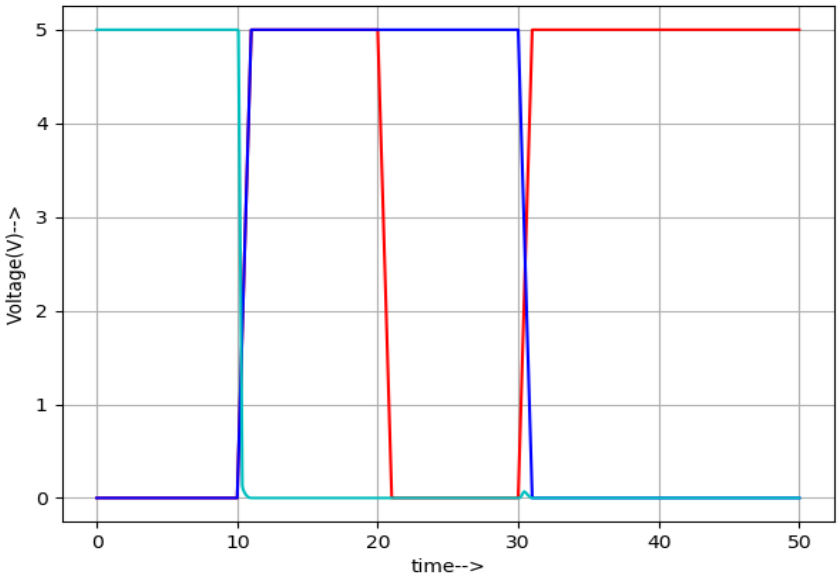
The truth table of NOR logic gate given in below table.

| **A** | **B** | **Y** |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

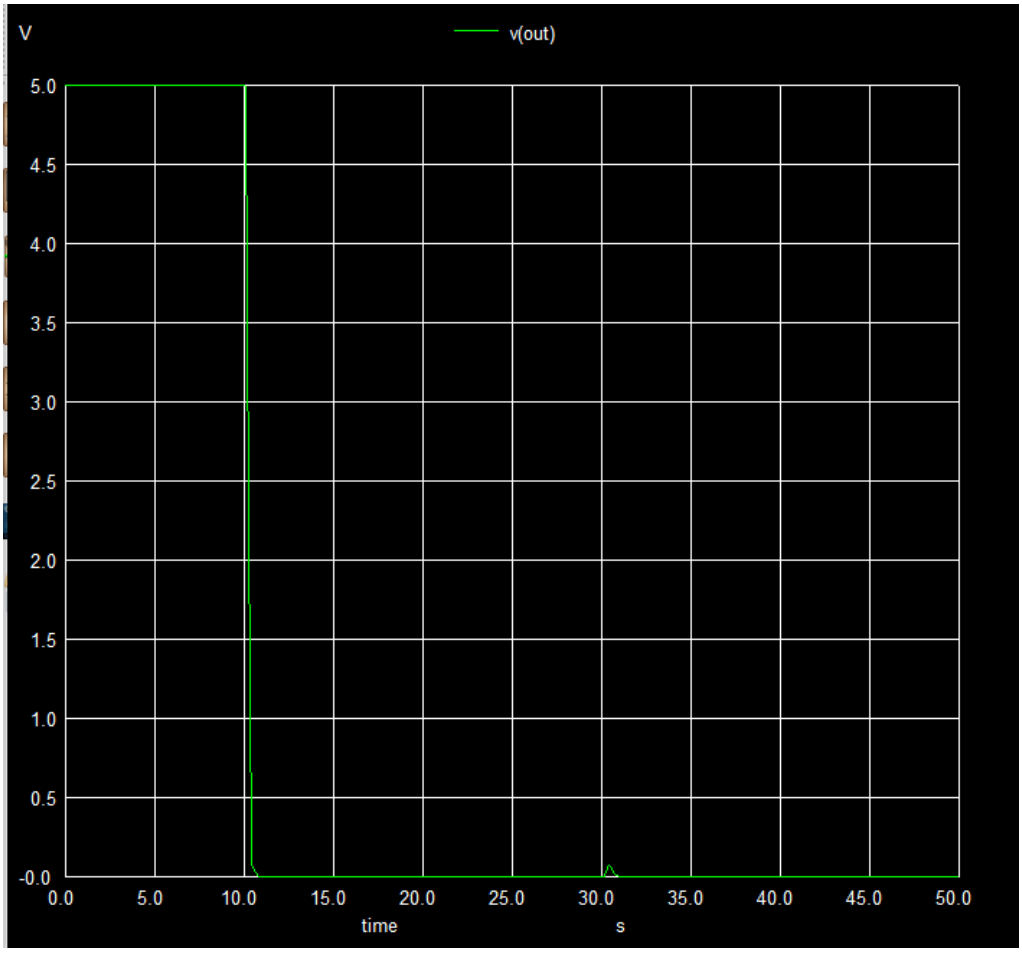
Logic Diagram of CMOS NOR gate




Schematic of NOR in ESIM




Results in python window




Results in Ngspice window

Conclusion: Hence we studied could make the schematic and test the working of CMOS NOR gate with two input and it is showing correct results.

Reference:https://www.elprocus.com/cmos-working-principle-and-applications/