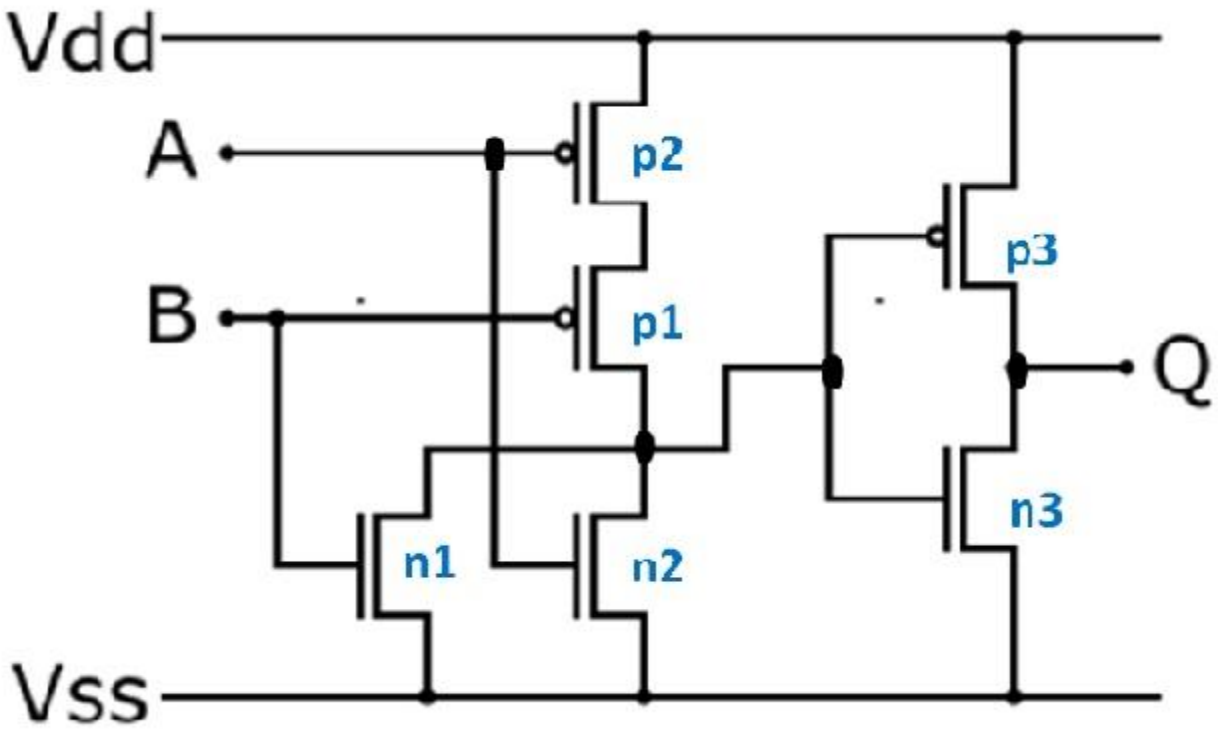
Experiment No: 05

Problem Statement: Simulate Schematic of CMOS two input OR gate and do ERC and transient analysis.

Theory:

The circuit diagram shows the circuit diagram of Logic OR operation. The OR is make with NOR followed with inverter.



Logic Diagram of CMOS OR Gate

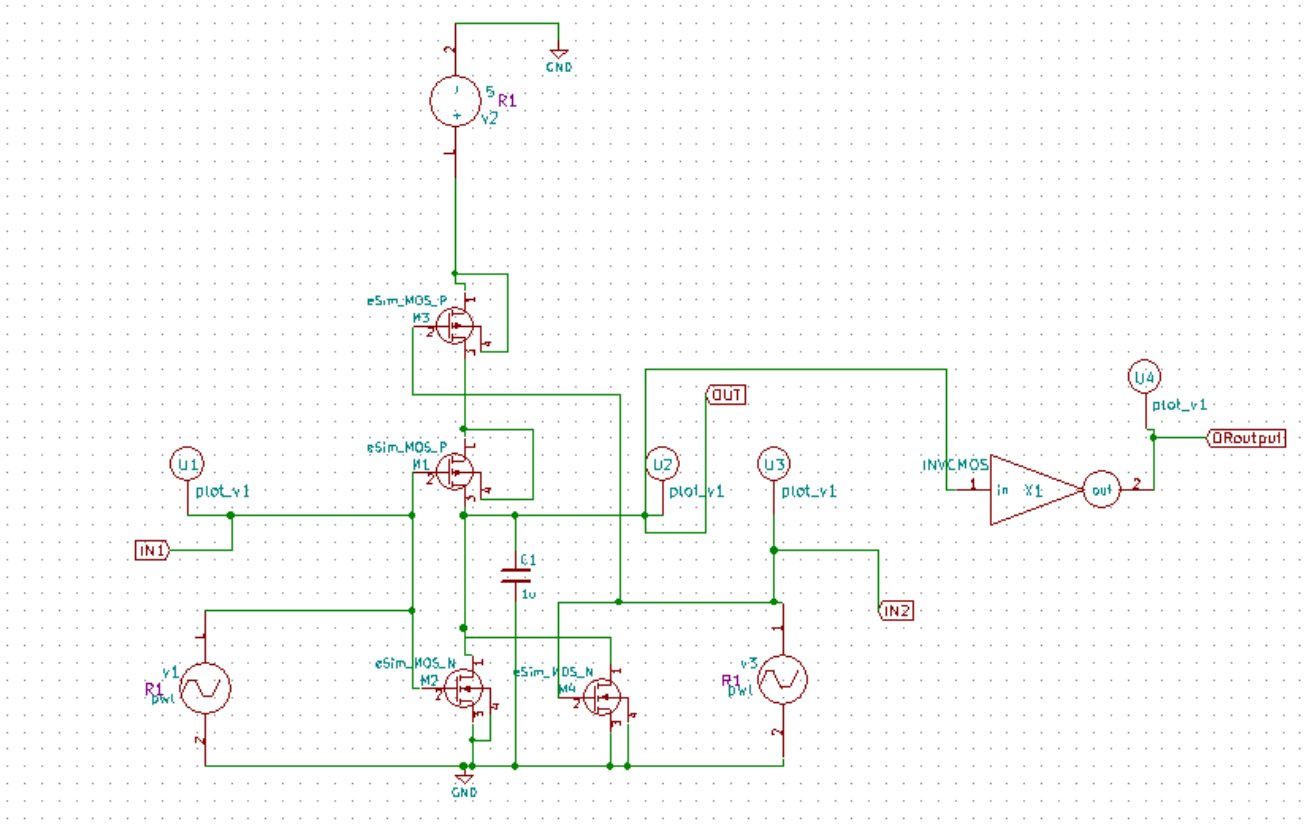
The two-input OR gate is built from four transistors. The parallel connection of the two n-channel transistors between GND and the output ensures that the gate-output is driven low (logical 0) when either gate input A or B is high (logical 1) and series P channel transistors between Vdd and output terminal ensures that the output is driven low (logical 1) when either gate input A or B is low (logical 0). The inverter in the end inverts the output and hence the net result is the logical OR function:

OR gate Truth table:

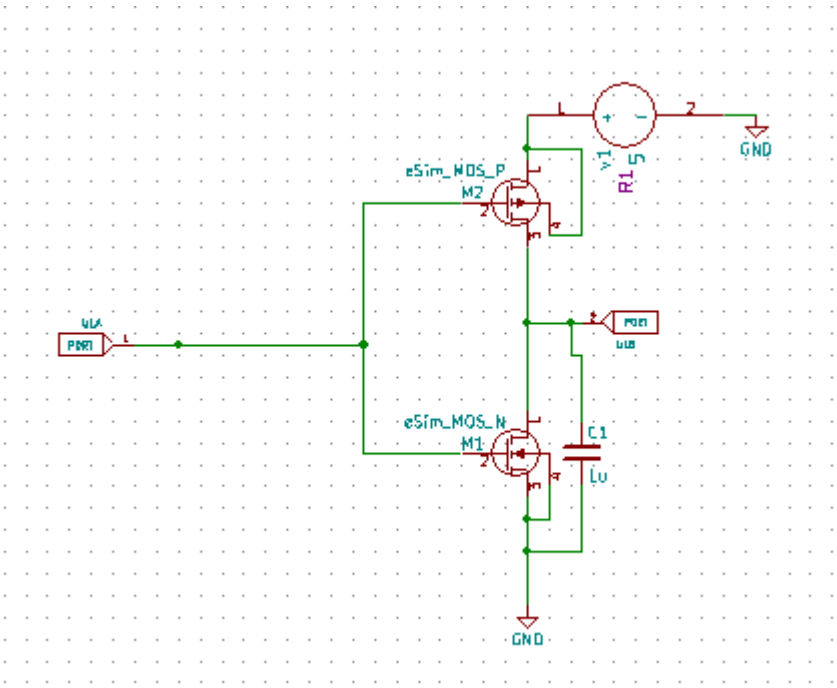
OR2

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

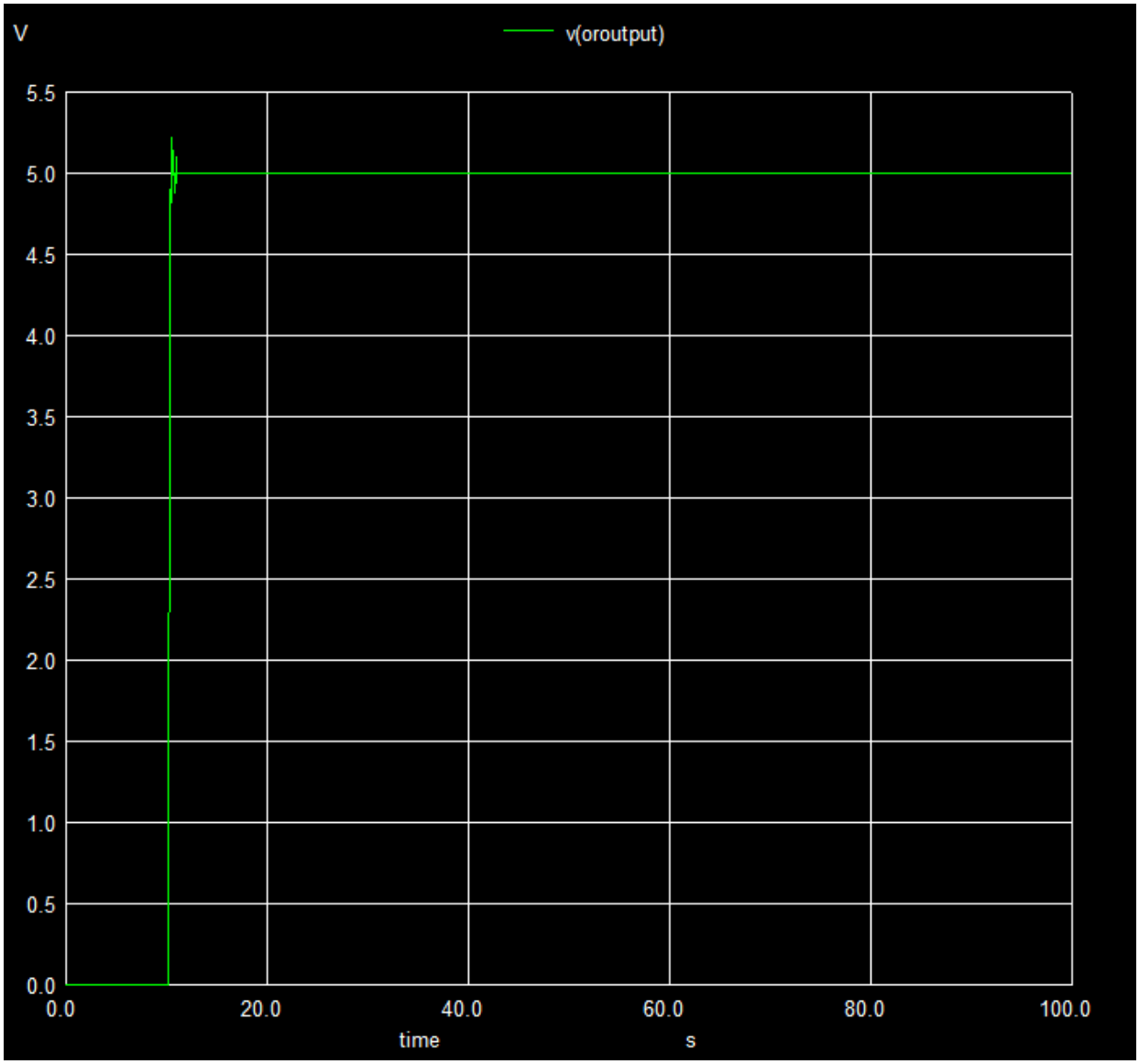
These type of logic gates are used in generation of parity generation and checking units. The two diagrams below shows the even and odd parity generator circuits respectively for a four data. With the help of these gates parity check operation can be also performed.



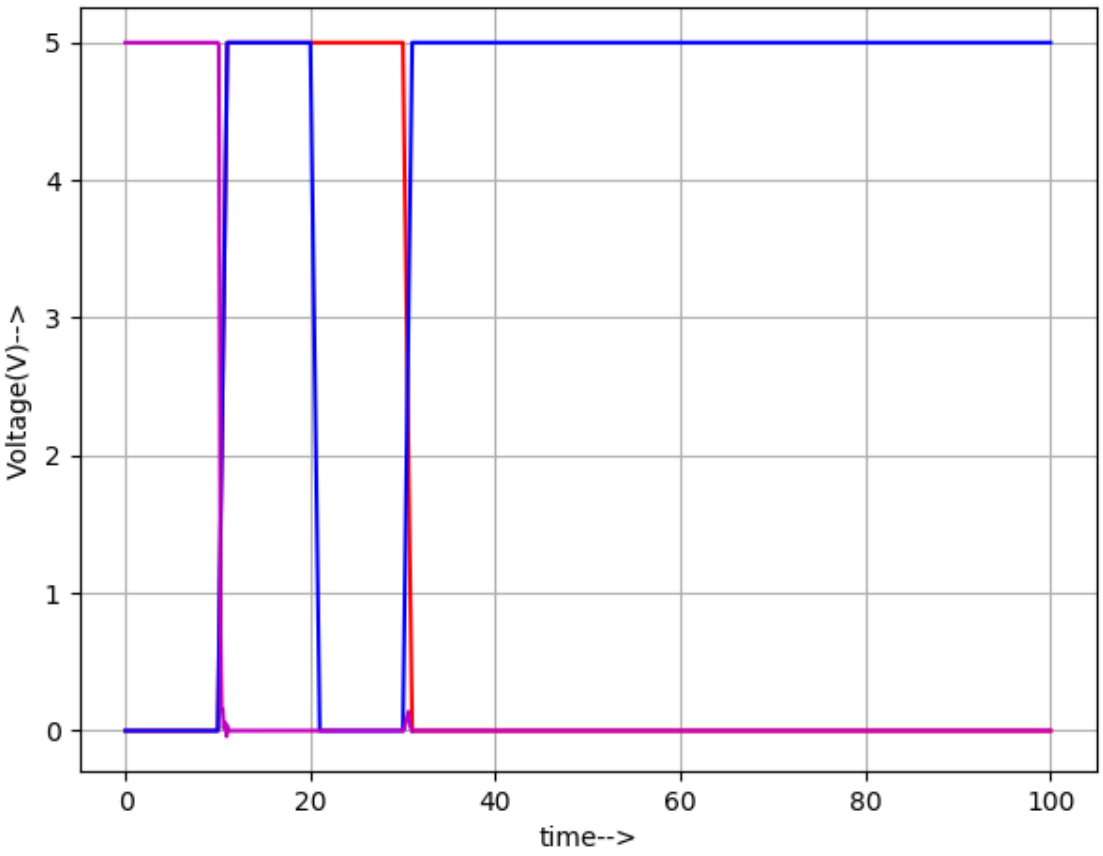
Schematic of sub-circuit of CMOS OR



Schematic of sub-circuit of CMOS Inverter



Results in Ngspice window



Results in python window

Conclusion: Hence we studied could make the schematic and test the working of CMOS OR gate with two input and it is showing correct results.

Reference: https://www.chegg.com/homework-help/questions-and-answers/study-cmos-circuit-fill-truth-table-circuit-b-0-0-0-1-1-0-1-1-q2975212