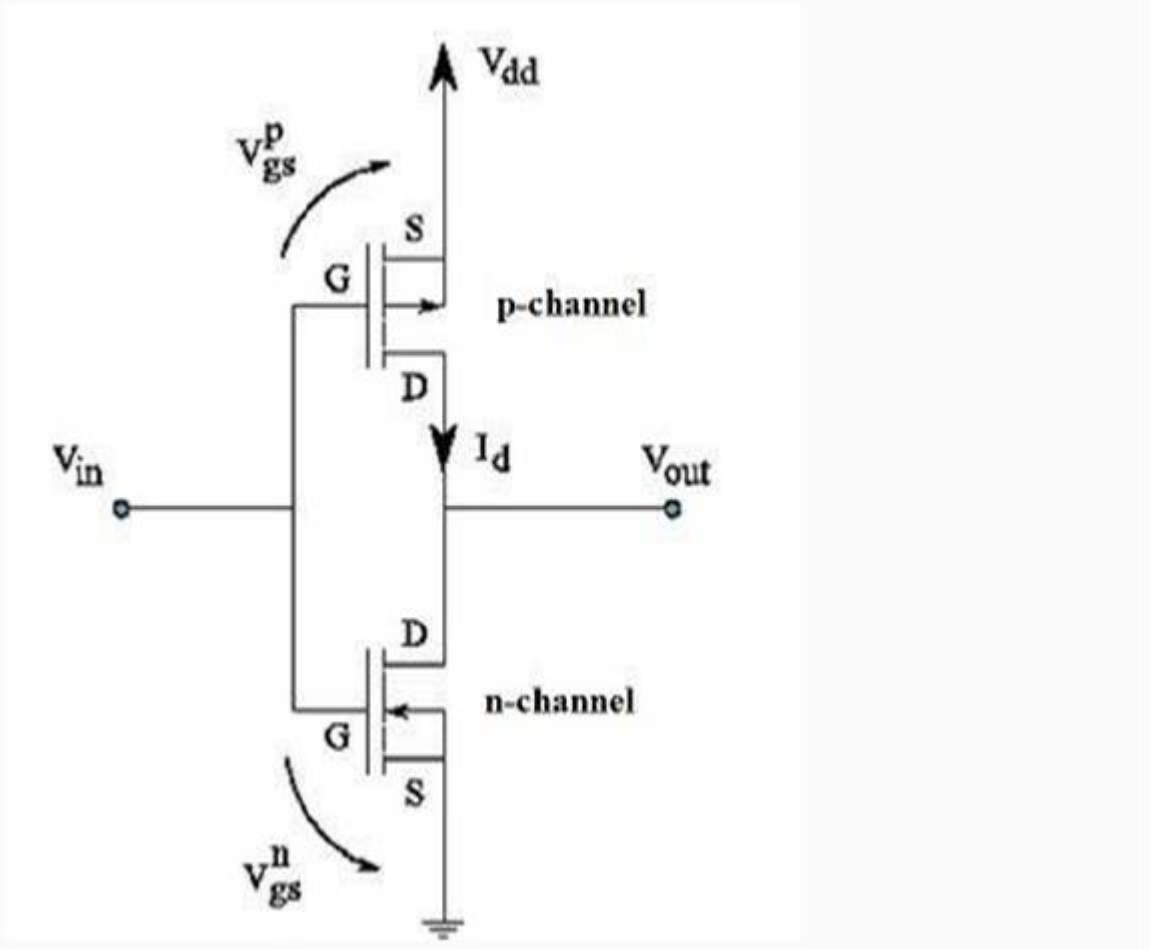
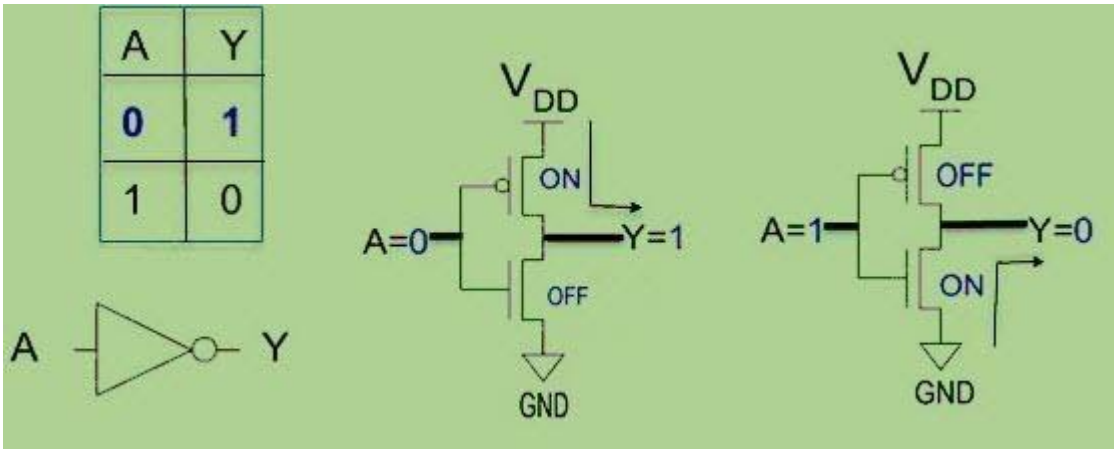
Experiment No: 01

Problem statement: Simulate Schematic of CMOS inverter and do ERC and transient analysis.

Circuit daigram:



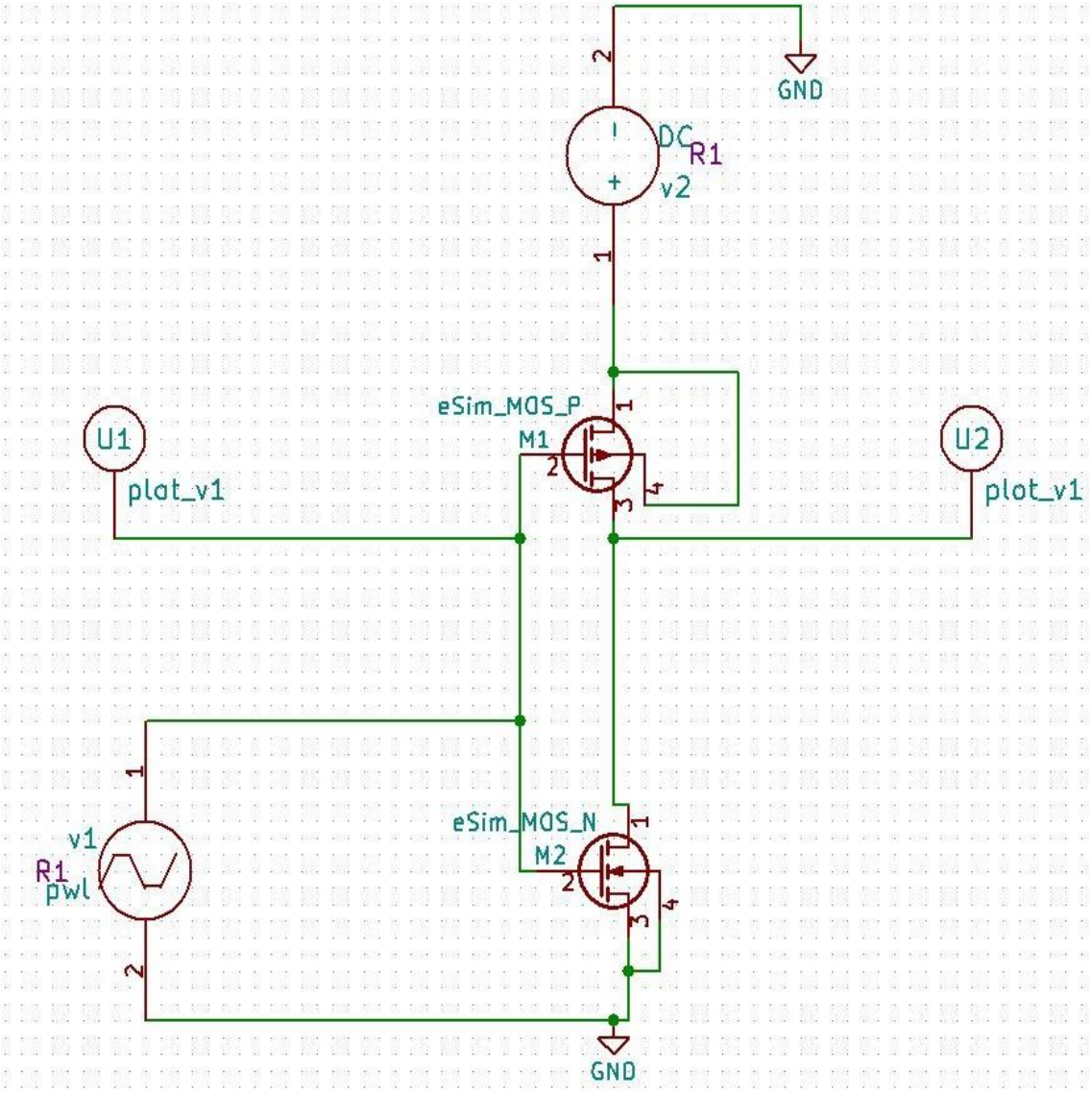
Theory: The inverter circuit as shown in the figure below. It consists of PMOS and NMOS FET. The input A serves as the gate voltage for both transistors.



CMOS Inverter

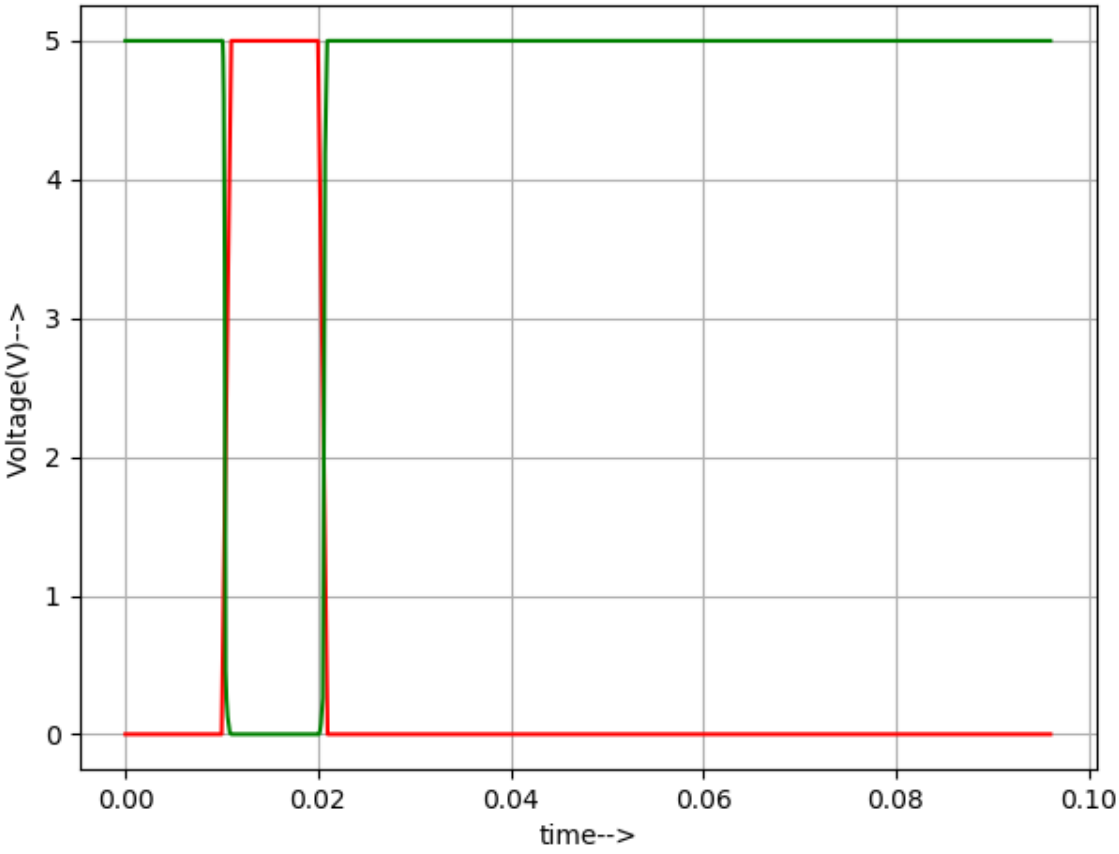
The NMOS transistor has an input from Vss (ground) and PMOS transistor has an input from Vdd. The terminal Y is output. When a high voltage (~ Vdd) is given at input terminal (A) of the inverter, the PMOS becomes open circuit and NMOS switched OFF so the output will be pulled down to Vss

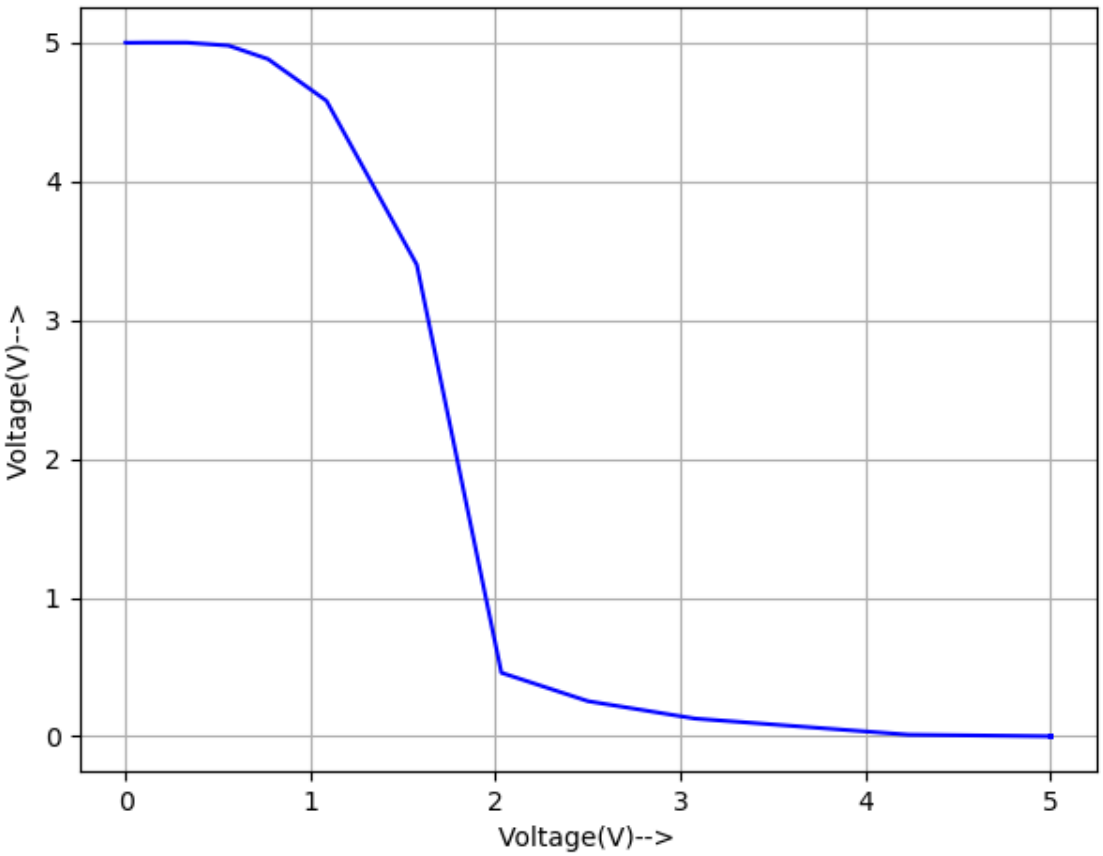
When a low-level voltage (<Vdd, ~0v) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes Vdd or the circuit is pulled up to Vdd.



Schematic of Cmos Inverter

INPUT	LOGIC INPUT	OUTPUT	LOGIC OUTPUT
0 v	0	Vdd	1
Vdd	1	0 v	0


5
4
3
2
1
0
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
time-->



Result in Python window

Conclusion: Hence we studied could make the schematic and test the working of CMOS Inverter and it is showing correct results.

Reference: https://www.elprocus.com/cmos-working-principle-and-applications/