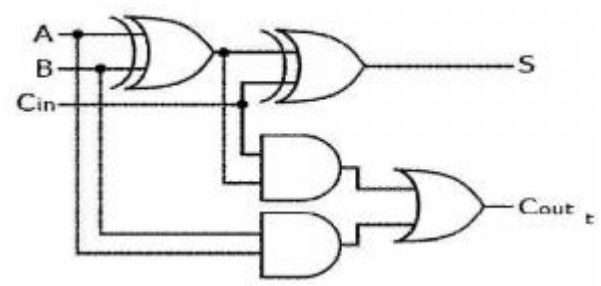
Experiment No: 08

Problem Statement: Simulate Schematic of CMOS full adder and do ERC and transient analysis.

Circuit diagram:



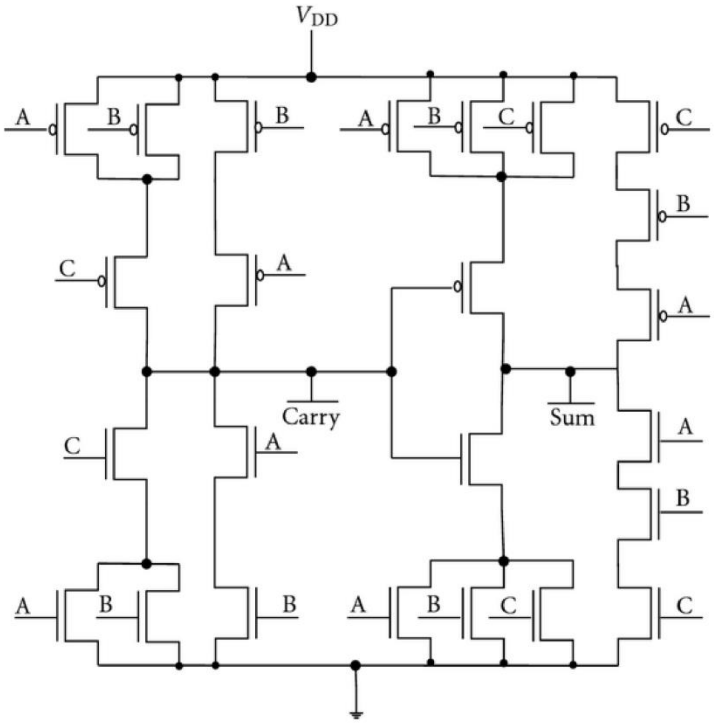
Full adder logic diagram

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table of full adder

Theory:

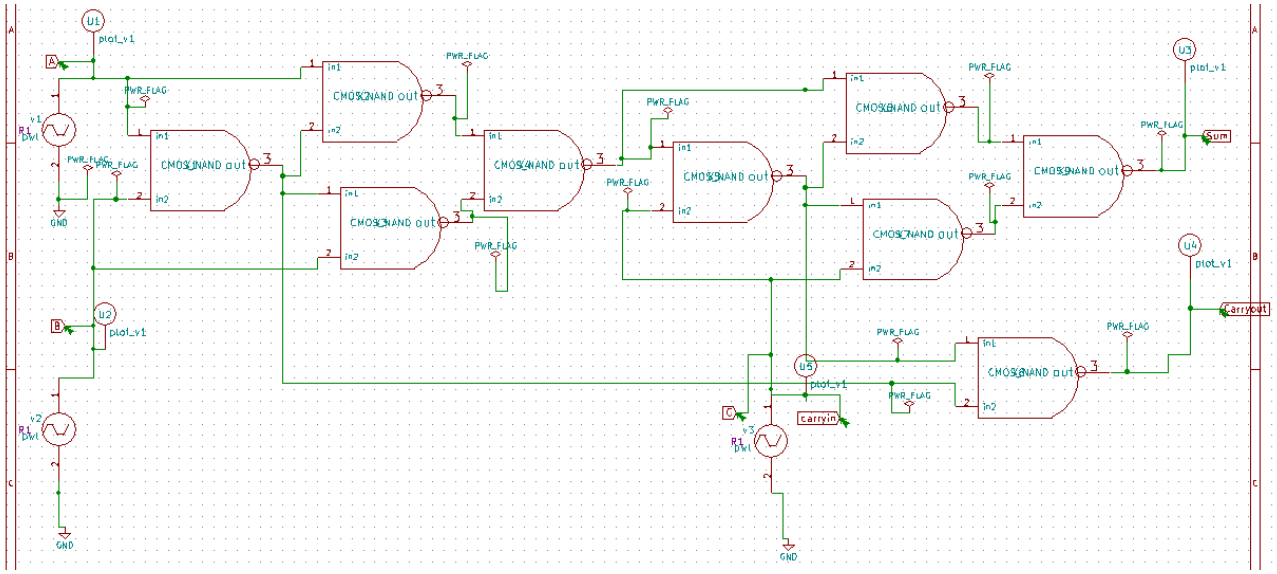
Full adder adds the incoming inputs and gives the result along with a carry. A 1-bit full adder takes three inputs and gives two outputs which are sum and carry. A full adder contains two half adders which are being connected to input A and B of one half adder and other is being connected to sum (output)which have the one input as Cin and other is the output of XNOR table(2). The arithmetic operations in multipliers, compressors, large adders, comparators and parity checks are done by full adder which is the fundamental unit in the above circuits, which also reduces the power consumption



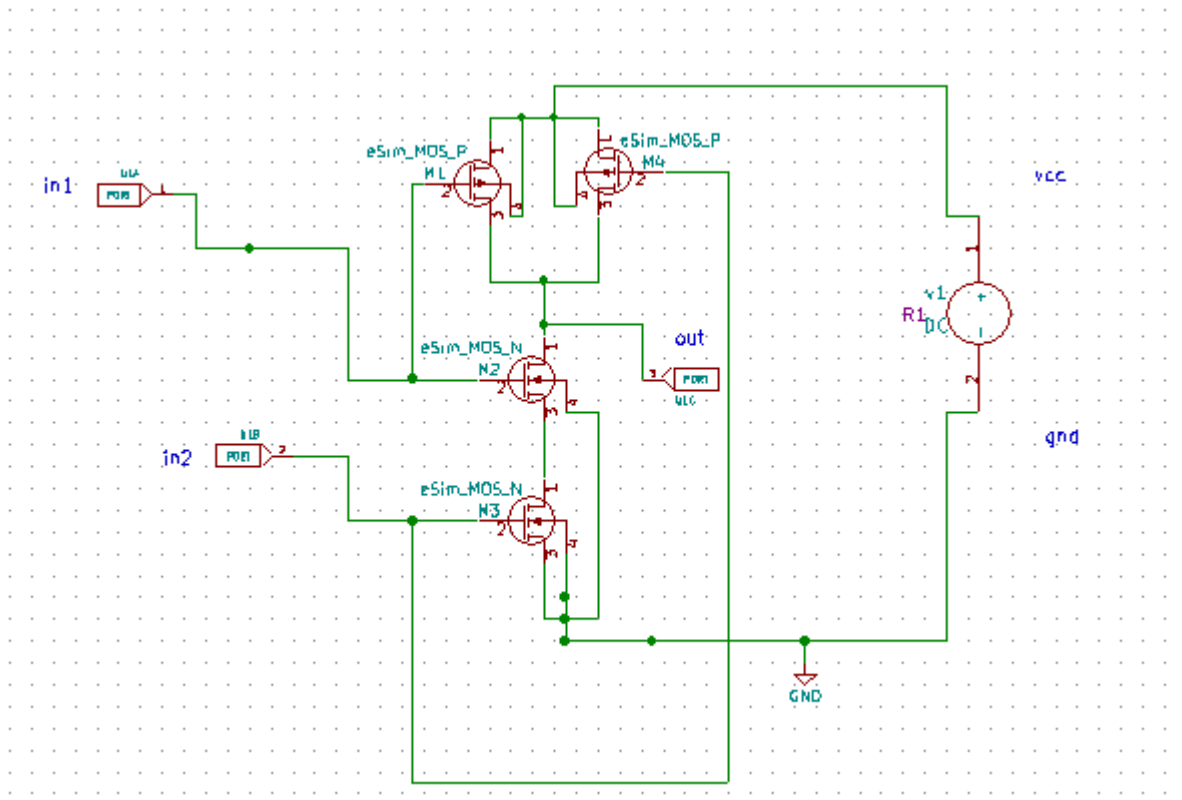
CMOS full adder circuit

Theory:

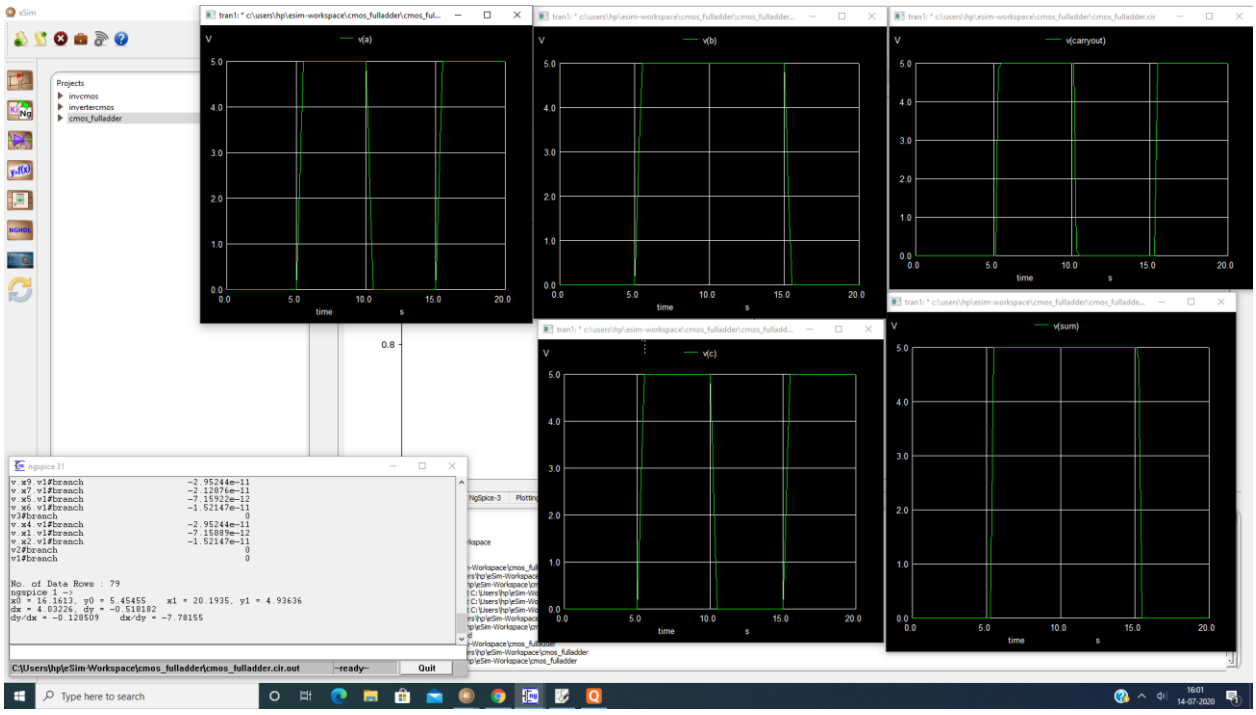
Full adder is a digital circuit that adds three binary number out of them one is input, carry and outputs sum and output carry. In cascaded of form it can be used to add two binary nos. It is used in ALU in processor chip to perform arithmetic and logical operations.



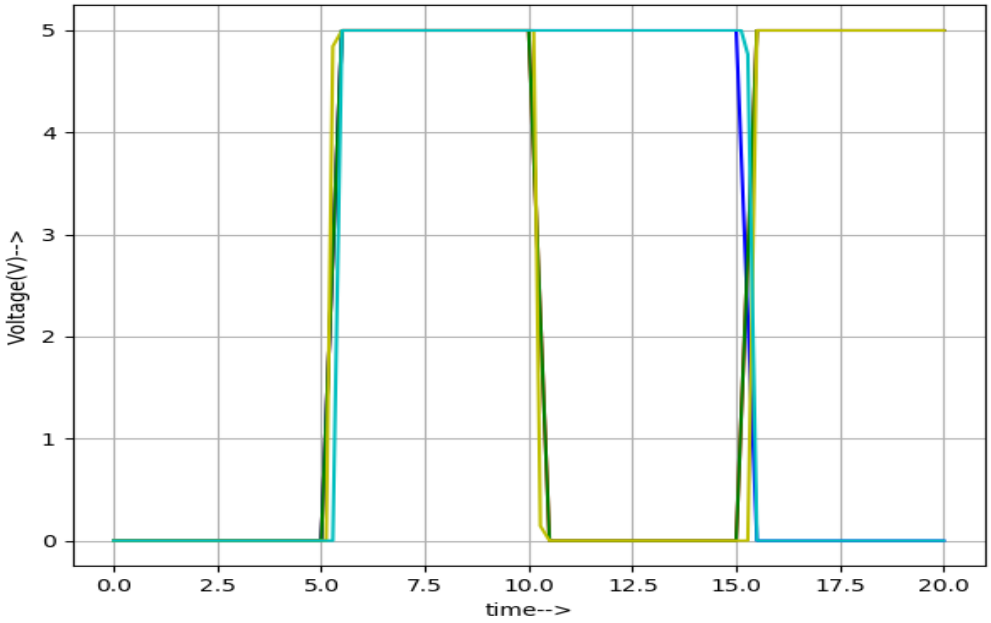
Schematic of Full adder using CMOS nand sub-circuit



Schematic of CMOS nand sub-circuit



Result in Ngspice window



Result in Python Window

Conclusion: Hence we studied could make the schematic and test the working of CMOS fulladder and it is showing correct results.

Reference:https://www.researchgate.net/figure/Conventional-CMOS-full-adder_fig1_249567605