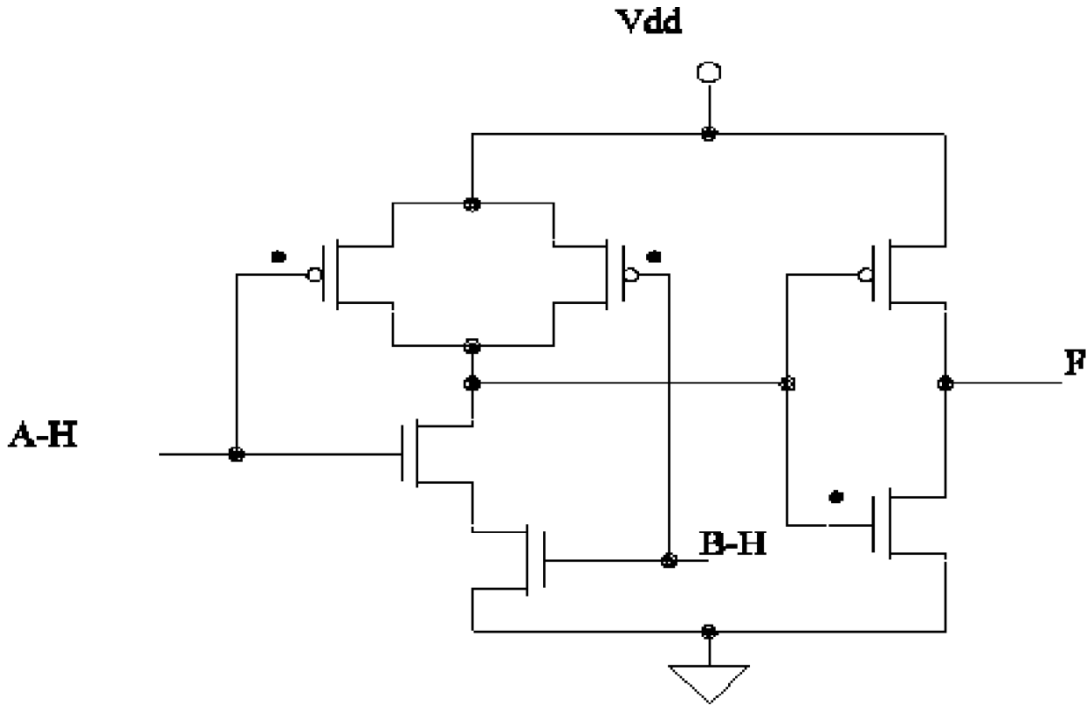
Experiment No: 06

Problem Statement: Simulate Schematic of CMOS two input AND gate and do ERC and transient analysis.



Logic Diagram of CMOS AND gate

Theory: AND gate is constructed from the NAND followed by a standard static inverter.

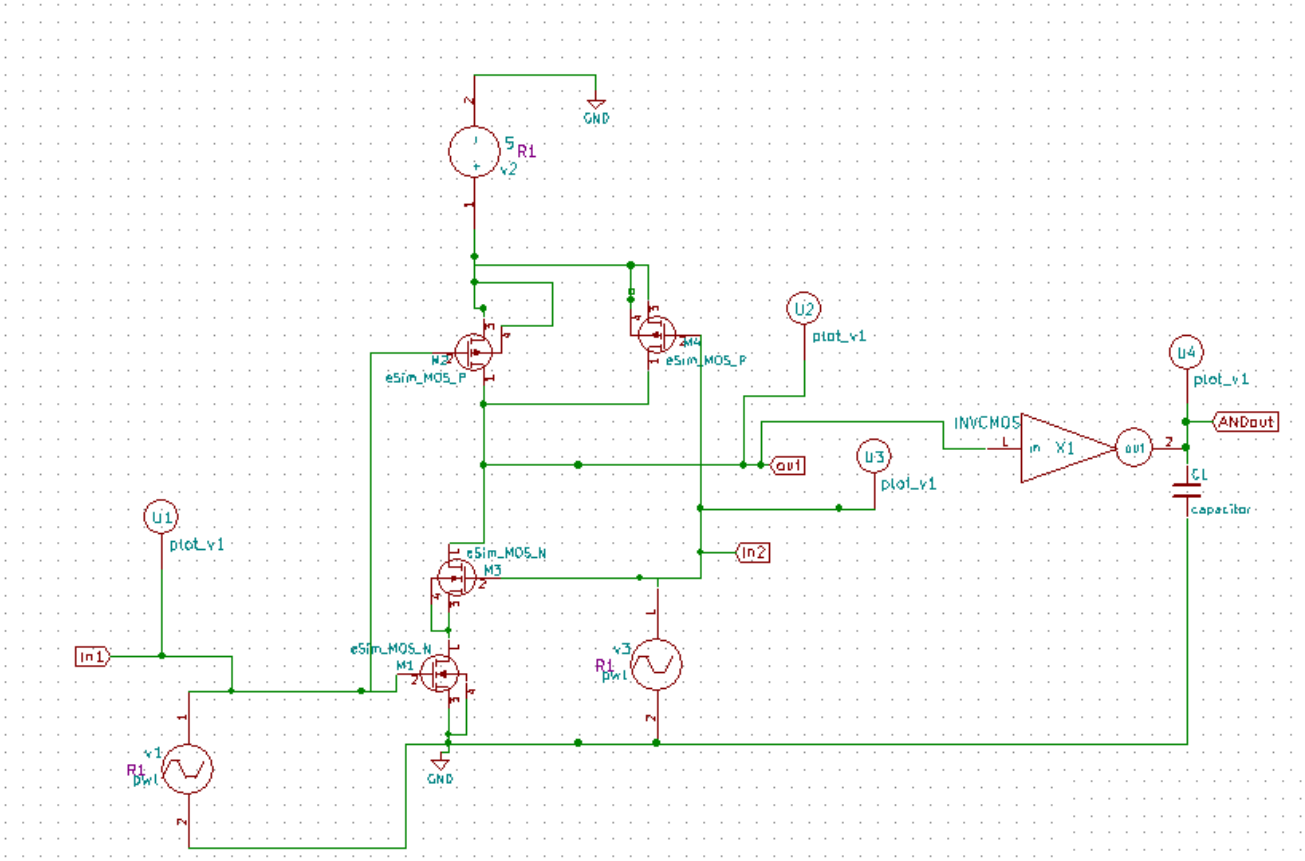
The two-input AND gate is built from four transistors. The series connection of the two n-channel transistors between GND and the output ensures that the gate-output is driven low (logical 0) when both gate input A or B is high (logical 1) and parallel P channel transistors between Vdd and output terminal ensures that the output is driven high (logical 1) when either gate input A or B is low (logical 0). The inverter in the end inverts the output and hence the net result is the logical AND function.

Truth table of AND Gate:

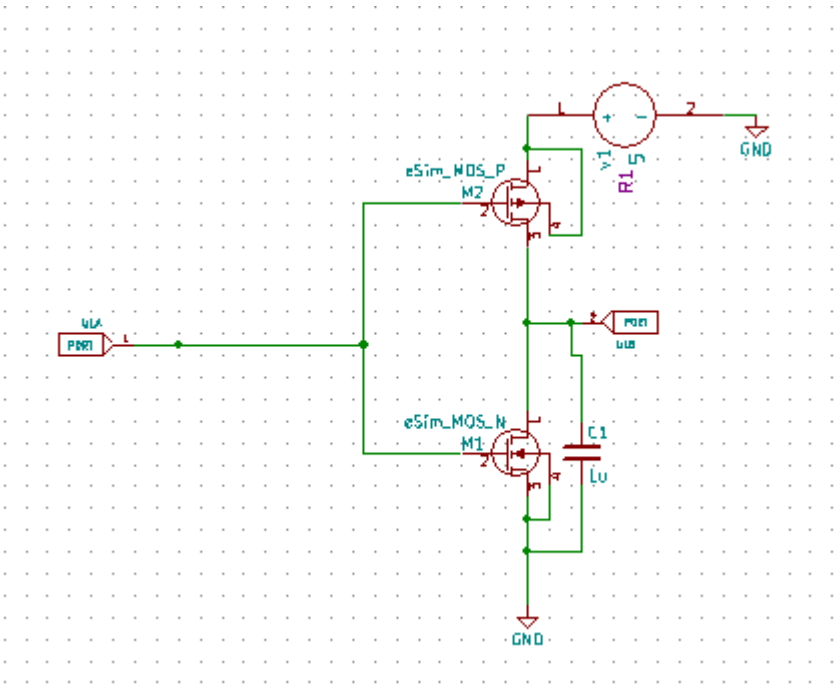
AND2

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

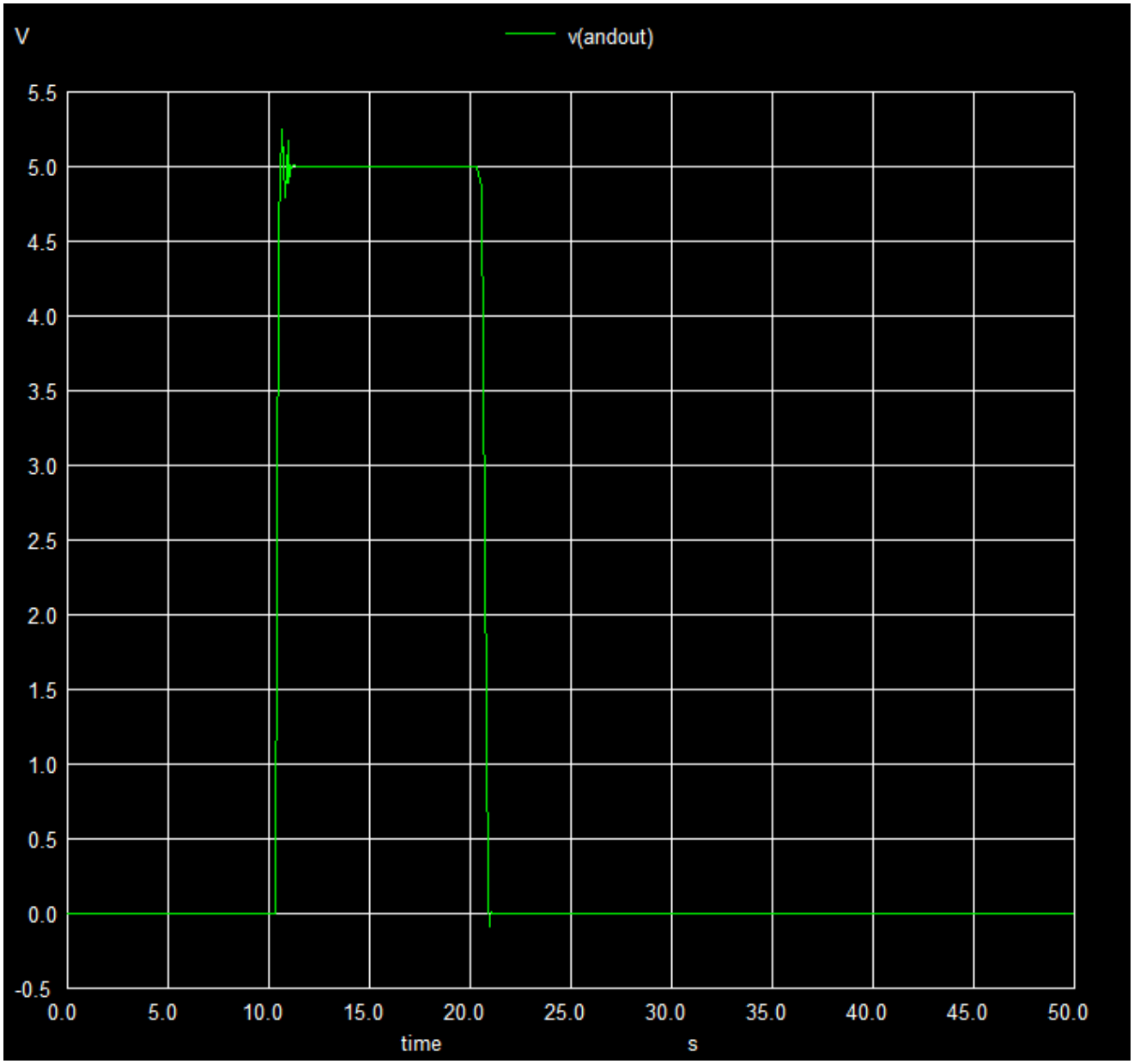
There are mainly two applications of AND gate as Enable gate and Inhibit gate. Enable gate means allowance of data through a channel and Inhibit gate is just the reverse of that process i.e. disallowance of data through a channel.

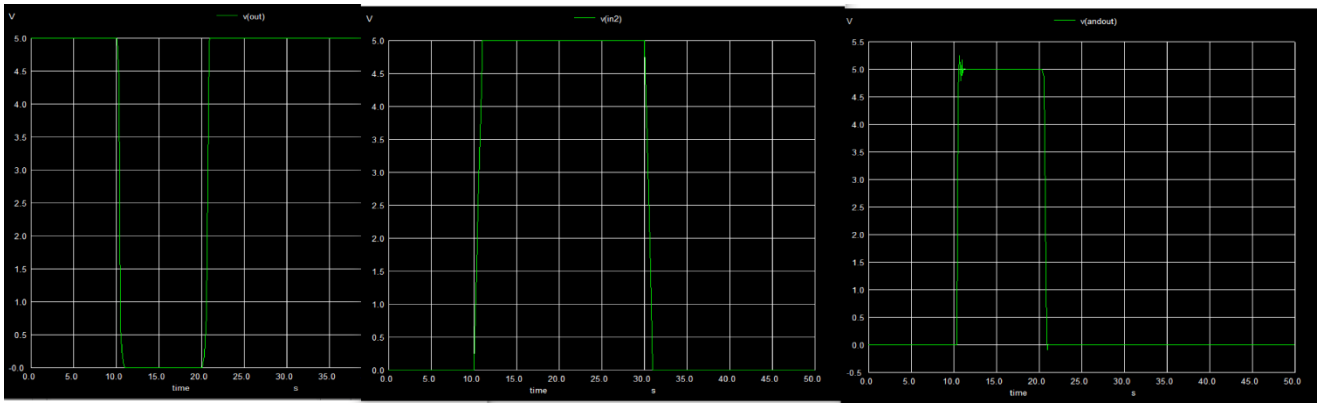


Schematic of AND circuit

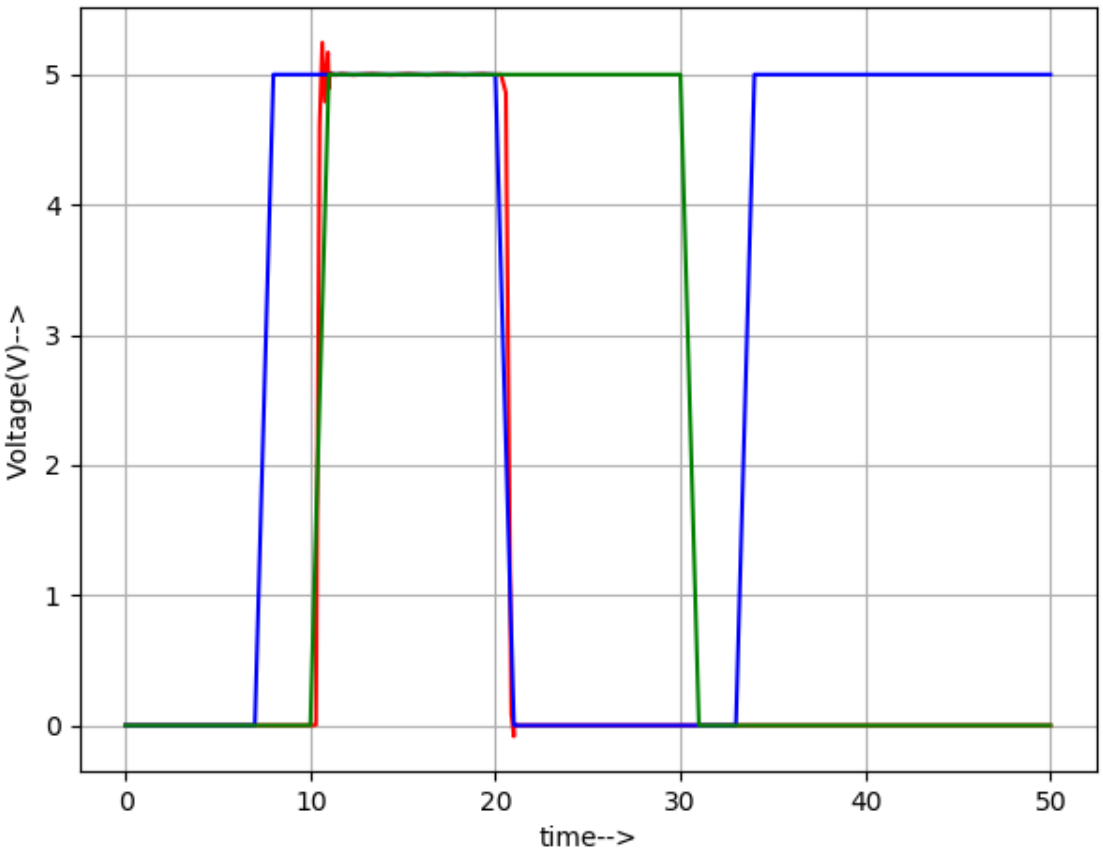


Schematic of sub-circuit Inverter





Result in Ngspice window



Result in python window

Conclusion: Hence we studied could make the schematic and test the working of CMOS AND gate with two input and it is showing correct results.

Reference: http://tiij.org/issues/issues/spring97/electronics/cmos/cmostran.html