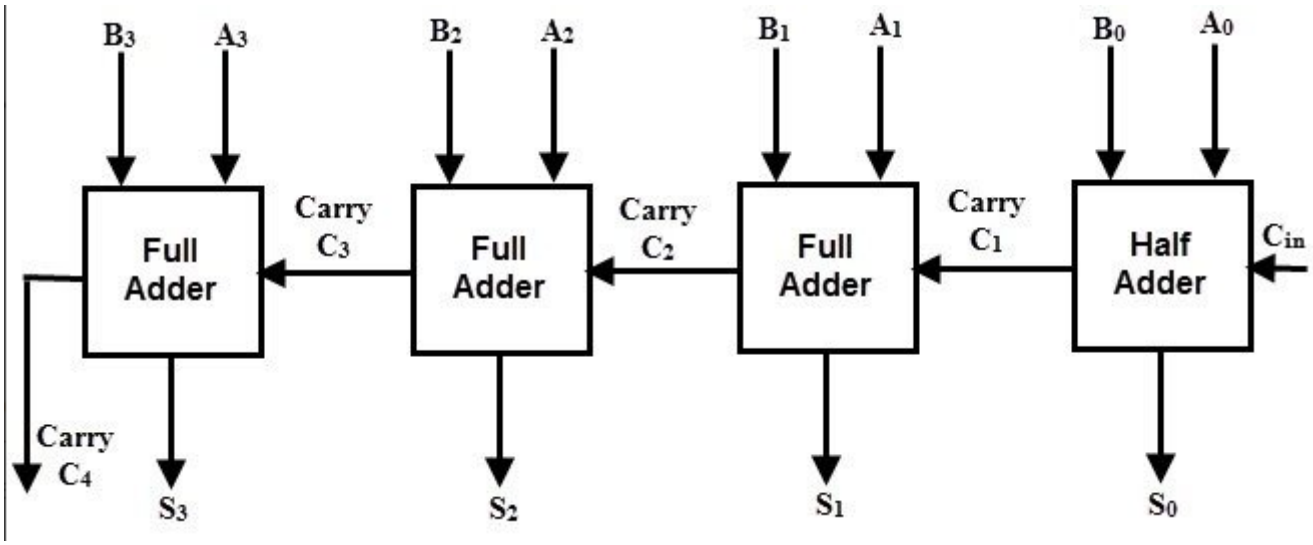
Experiment No: 09

Problem Statement: Simulate Schematic of CMOS 4 bit full adder and do ERC and transient analysis.

Circuit diagram:

4 bit full adder circuit



4 Bit Full adder Logic Diagram using 2 bit full adder

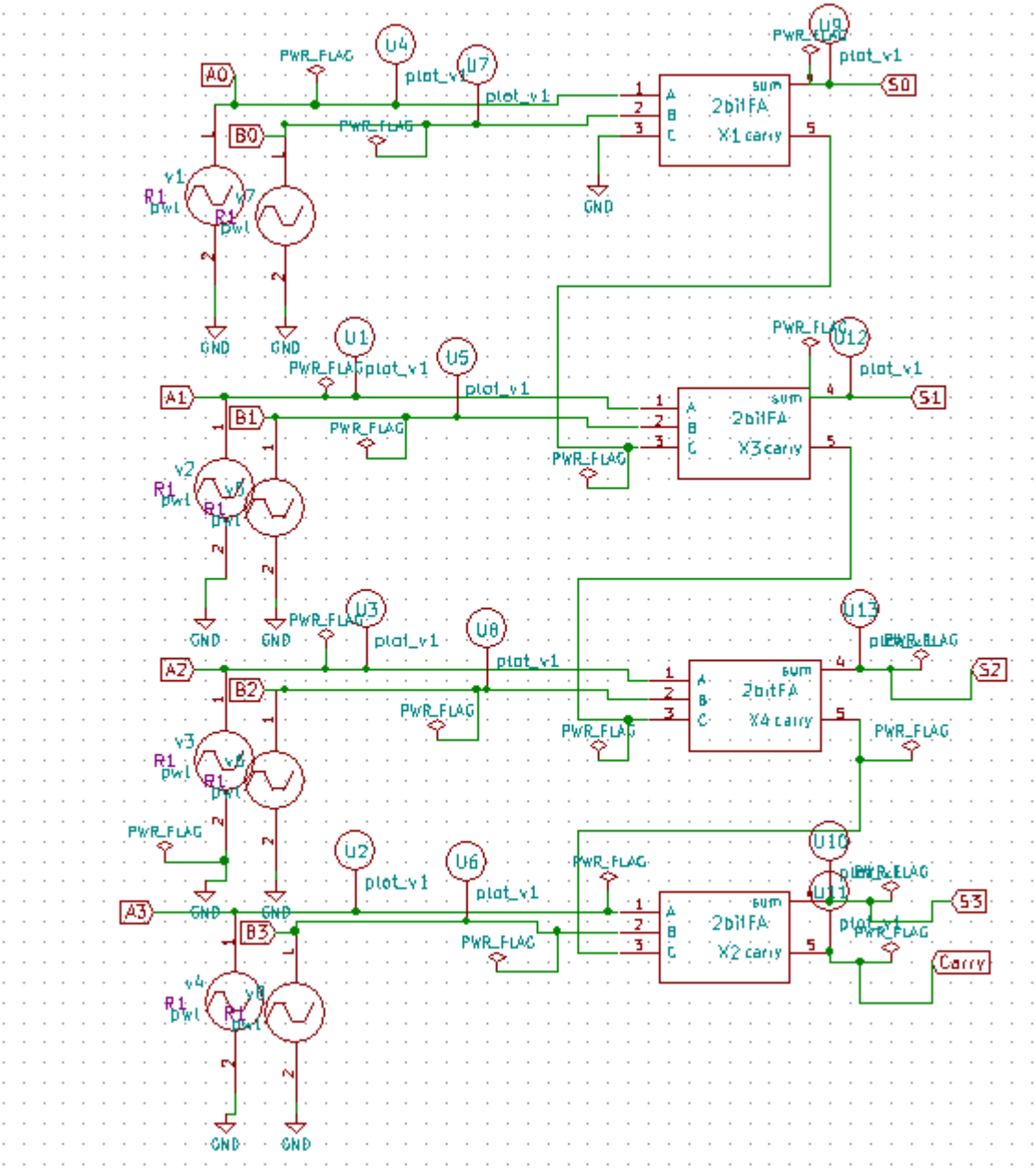
Theory:

The design was first carried out for 1 bit after which extended for 4 bit also. Performance parameters such as power, delay and area were compared with the existing designs such as complementary pass-transistor logic, transmission gate adder, transmission function adder with static CMOS output drive full adder.

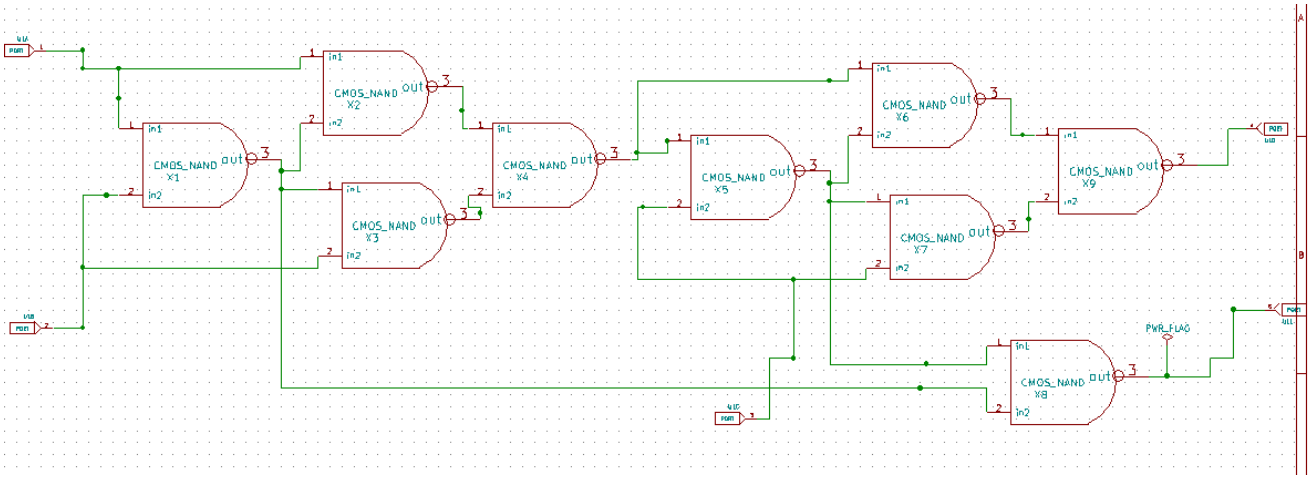
Truth table: 4 Bit full adder

Input Data A				Input Data B				Addition				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1
1	0	0	0	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0
1	0	1	0	1	0	1	1	1	0	0	1	0
1	1	1	0	1	1	1	1	1	1	0	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1

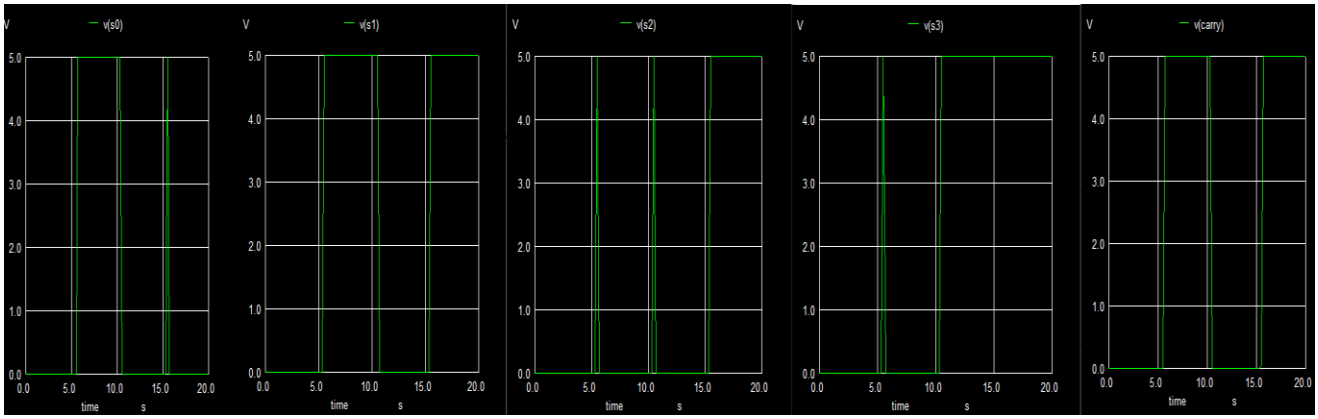
Adder and subtractor are basically used for performing arithmetical functions like addition, subtraction, multiplication and division in electronic calculators and digital instruments. They are also used in microcontrollers for arithmetic additions, PC (program counter) and timers.



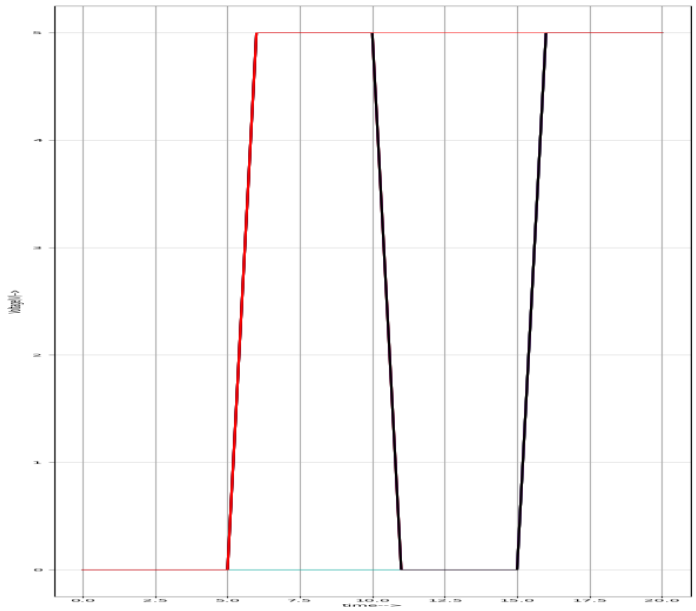
Schematic of 4 bit full Adder using subcircuit 2 bit full adder



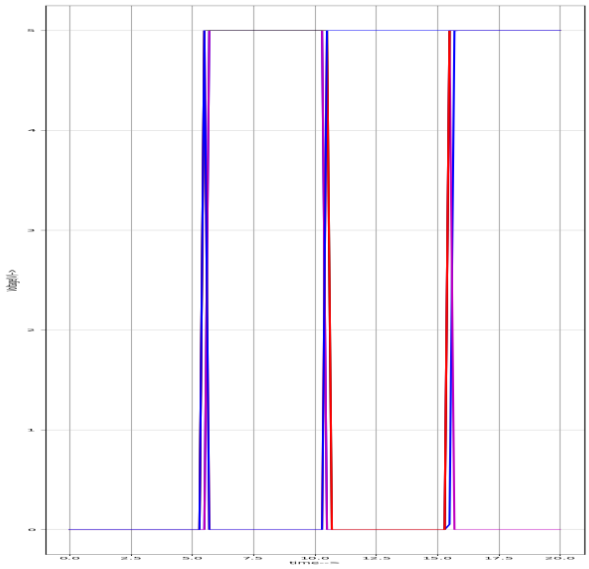
Schematic of subcircuit 2 bit full adder



Result in ngspice window



Result in python window(Input)



Result in python window(output)

Conclusion: Hence we studied could make the schematic and test the working of CMOS 4 bit fulladder and it is showing correct results.

Reference:https://ijcsmc.com/docs/papers/July2017/V6I7201748.pdf