EXPERIMENT NO: 10

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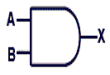
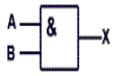
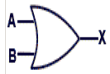
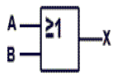
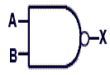
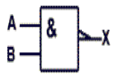
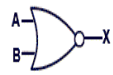
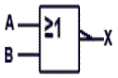
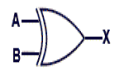
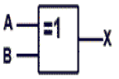
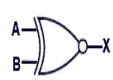
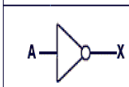
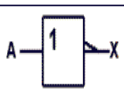
Aim of the Experiment:

Analysis of basic gates using eSim.

Theory:

There are seven types of logic gates, called AND, OR, NAND (Not AND), NOR (Not OR), XOR (Exclusive OR) XNOR (Exclusive NOR) and NOT. Please se the table below for more details of each gate:

ANSI Symbol	IEC Symbol	Description	Boolean
		The AND gate output is at logic 1 when, and only when all its inputs are at logic 1, otherwise the output is at logic 0.	$X = A \cdot B$
		The OR gate output is at logic 1 when one or more of its inputs are at logic 1. If all the inputs are at logic 0, the output is at logic 0.	$X = A + B$
		The NAND Gate output is at logic 0 when, and only when all its inputs are at logic 1, otherwise the output is at logic 1.	$X = \overline{A \cdot B}$
		The NOR gate output is at logic 0 when one or more of its inputs are at logic 1. If all the inputs are at logic 0, the output is at logic 1.	$X = \overline{A + B}$
		The XOR gate output is at logic 1 when one and ONLY ONE of its inputs is at logic 1. Otherwise the output is logic 0.	$X = A \oplus B$
		The XNOR gate output is at logic 0 when one and ONLY ONE of its inputs is at logic 1. Otherwise the output is logic 1. (It is similar to the XOR gate, but its output is inverted).	$X = \overline{A \oplus B}$
		The NOT gate output is at logic 0 when its only input is at logic 1, and at logic 1 when its only input is at logic 0. For this reason it is often called an INVERTER.	$X = \overline{A}$

Procedure:

1. Create the schematic of the Basic Gtaes as shown in Figure-1.
2. Annotate the schematic.
3. Test Electric rules.
4. Generate the netlist.
5. Insert analysis for transient analysis from 0 to 30 us with a step time of 10 us.
6. Insert Source Details.
7. Insert values for Ngspice Models.
8. Convert KiCad netlist to Ngspice netlist.
9. Simulate the Ngspice netlist using Ngspice simulator.

Source Parameters:

Following are the Pulse input parameters for V1:

1. Enter Initial Value - 5
2. Enter Pulsed Value - 0
3. Enter Delay Time - 0.1u
4. Enter Rise Time - 0.1u
5. Enter Fall Time - 0.1u
6. Enter Pulse Width - 2u
7. Enter Period - 20u

Following are the Pulse input parameters for V2:

1. Enter Initial Value - 0
2. Enter Pulsed Value - 5
3. Enter Delay Time - 0.1u
4. Enter Rise Time - 0.1u
5. Enter Fall Time - 0.1u
6. Enter Pulse Width - 2u
7. Enter Period - 20u

Schematic Diagram:

The circuit schematic of basic gates in eSim is as shown below:

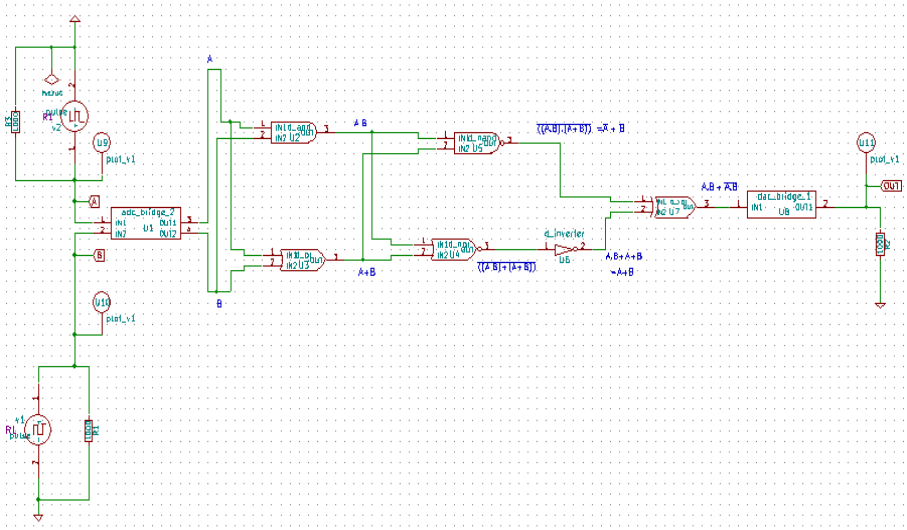


Figure 1: Basic gates

Simulation Results:

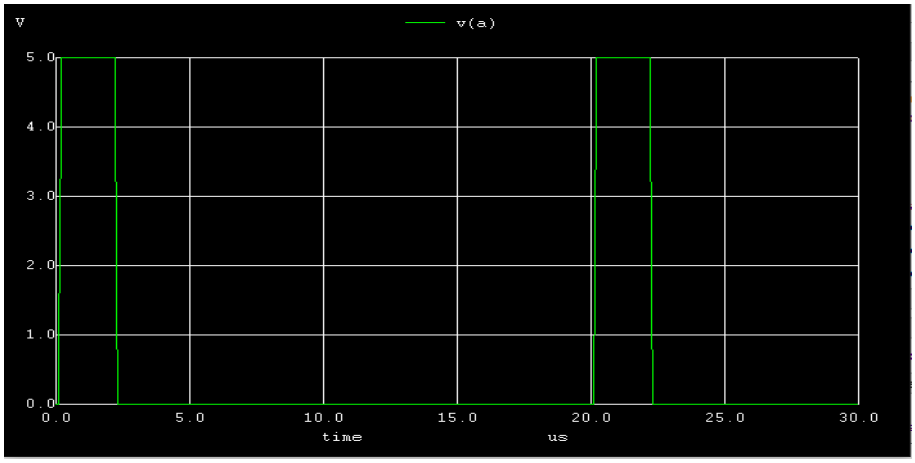


Figure 2: Ngspice Input-1 Plot

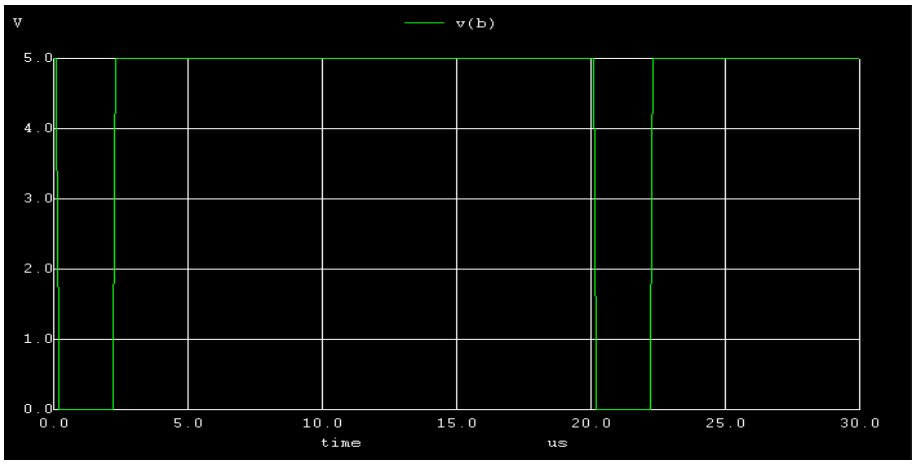


Figure 3: Ngspice Input-2 Plot

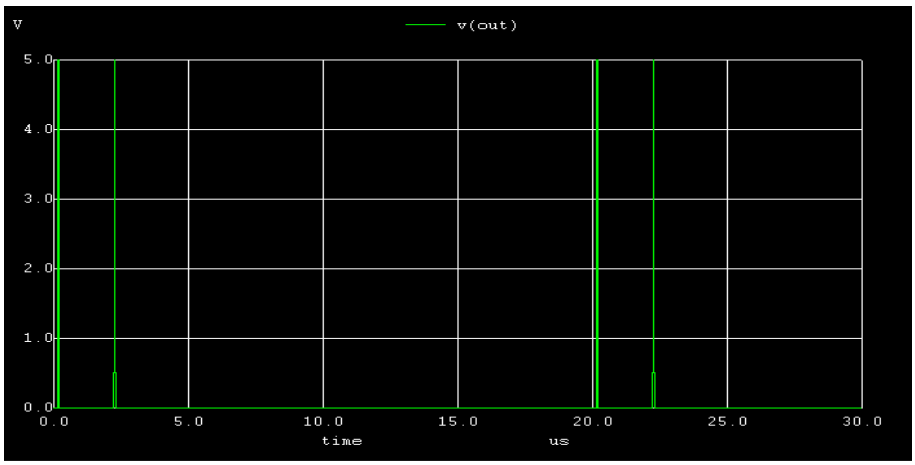


Figure 4: Ngspice Output Plot

Conclusion:

Thus, we have studied the basic gates using eSim and we get the appropriate waveforms.

References:

http://www.learnabout-electronics.org/Digital/dig21.php