EXPERIMENT NO: 15

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Date: March 16, 2016

Aim of the Experiment:

Analysis of PISO register using eSim.

Theory:

The Shift Register is type of sequential logic circuit that can be used for the storage or the transfer of data in the form of binary numbers. This sequential device loads the data present on its inputs and then moves or shifts it to its output once every clock cycle, hence the name shift register.

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins of the register. The data is then read out sequentially in the normal shift-right mode.

Procedure:

1. Create the schematic of the PISO Register as shown in Figure-1.
2. Annotate the schematic.
3. Test Electric rules.
4. Generate the netlist.
5. Insert analysis for transient analysis from 0 to 500 ms with a step time of 0.1 ms.
6. Insert Source Details.
7. Insert values for Ngspice Models.
8. Convert KiCad netlist to Ngspice netlist.
9. Simulate the Ngspice netlist using Ngspice simulator.

Source Parameters:

For DC Voltage Source (V1):

1. Enter Value for V1 - 0

Following are the Pulse input parameters for V2:

1. Enter Initial Value - 5
2. Enter Pulsed Value - 0
3. Enter Delay Time - 0
4. Enter Rise Time - 0
5. Enter Fall Time - 0
6. Enter Pulse Width - 48m
7. Enter Period - 96m

Following are the Pulse input parameters for V3:

1. Enter Initial Value - 5
2. Enter Pulsed Value - 0
3. Enter Delay Time - 0
4. Enter Rise Time - 0
5. Enter Fall Time - 0
6. Enter Pulse Width - 150m
7. Enter Period - 550m

For DC Voltage Source (V4):

1. Enter Value for V4 - 5

For DC Voltage Source (V5):

1. Enter Value for V5 - 0

Schematic Diagram:

The circuit schematic of PISO register in eSim is as shown below:

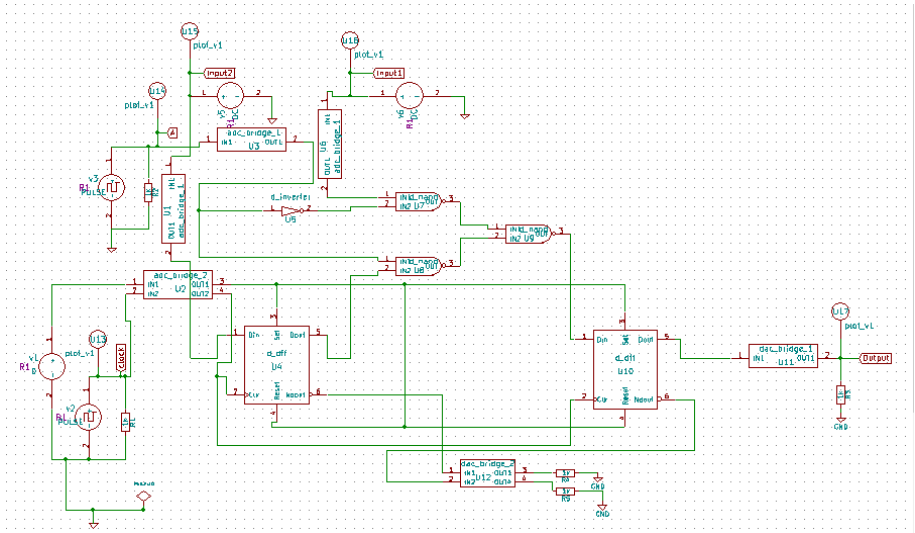

Figure 1: PISO Register

Simulation Results:

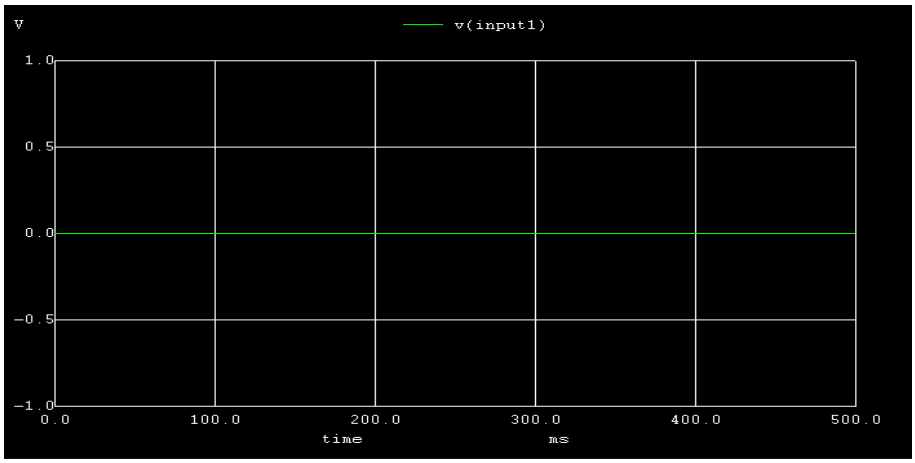

Figure 2: Ngspice Input-1 Plot

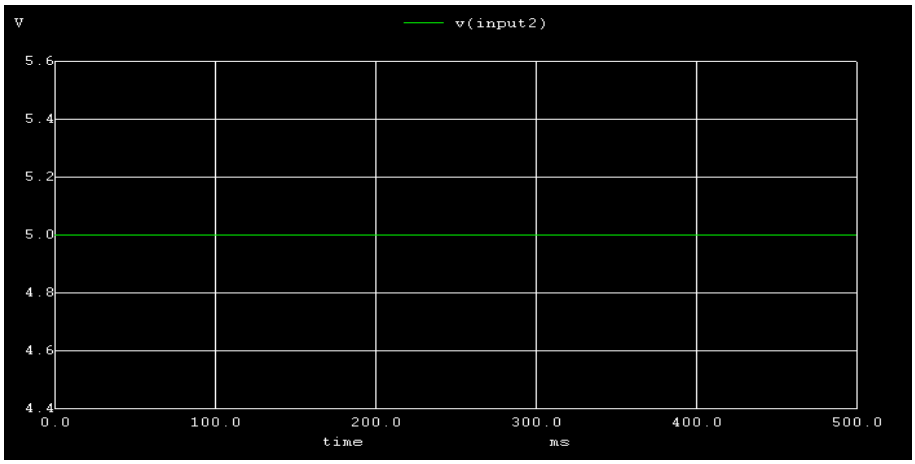

Figure 3: Ngspice Input-2 Plot

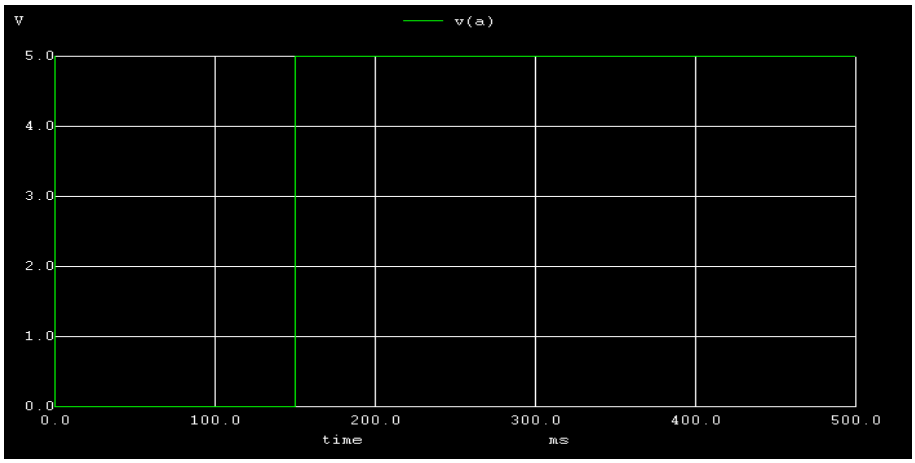

Figure 4: Ngspice Select Input Plot

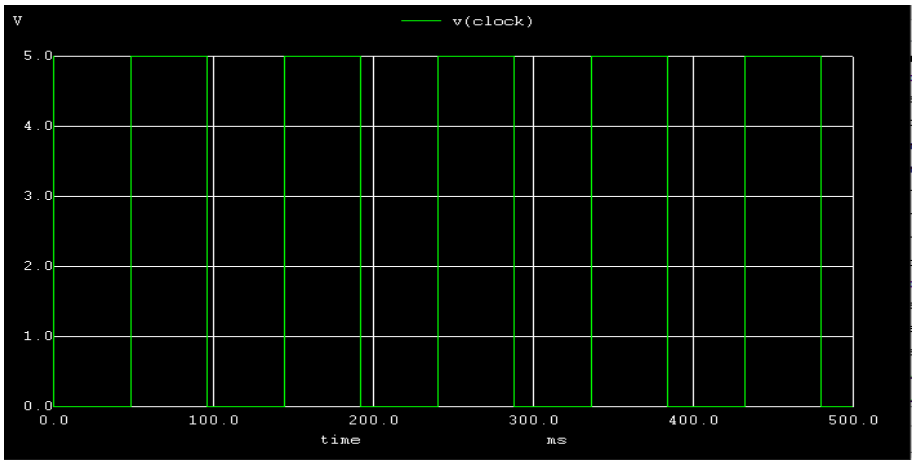

Figure 5: Ngspice Clock Input Plot

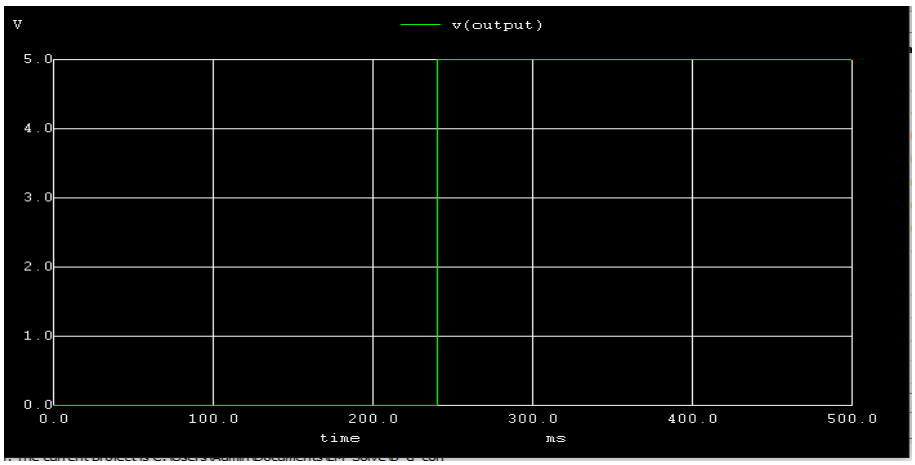

Figure 6: Ngspice Output Plot

Conclusion:

Thus, we have studied the PISO register circuit using eSim and we get the appropriate waveforms.

References:

http://www.electronics-tutorials.ws/sequential/seq-5.html