EXPERIMENT NO. - 3

Aim of the Experiment:

BJT bias circuit: Design, assemble and test.

Theory:

Biasing in electronics is the method of establishing predetermined voltages and currents at various points of an electronic circuit to set an appropriate operating point. The purpose of a biasing circuit is to establish an operating point for the BJT, which provides linear operation and good stability with regard to variations of temperature as well as manufacturing parameters (e.g. β). Since the operating point is a fixed point on the characteristics it is also known as bias point, quiescent point or simply Q-point. It is the point on the output characteristics that shows the collector-emitter voltage V_{CE} and the collector current I_C with no input signal applied. If a BJT is to be operated as an amplifier, the base emitter junction must be forward biased and the base collector junction must be reverse biased.

Active or Linear Region Operation

Base–Emitter junction is forward biased

Base–Collector junction is reverse biased

Cutoff Region Operation

Base–Emitter junction is reverse biased

Base–Collector junction is reverse biased

Saturation Region Operation

Base–Emitter junction is forward biased

Base–Collector junction is forward biased

Thermal considerations

At constant current, the voltage across the emitter–base junction V_{BE} of a bipolar transistor decreases 2 mV (silicon) and 1.8mV (germanium) for each 1 °C rise in temperature (reference being 25 °C). By the Ebers–Moll model, if the base–emitter voltage V_{BE} is held

constant and the temperature rises, the current through the base–emitter diode I_B will increase, and thus the collector current IC will also increase. Depending on the bias point, the power dissipated in the transistor may also increase, which will further increase its temperature and exacerbate the problem. This deleterious positive feedback results in thermal runaway. There are several approaches to mitigate bipolar transistor thermal runaway. For example,

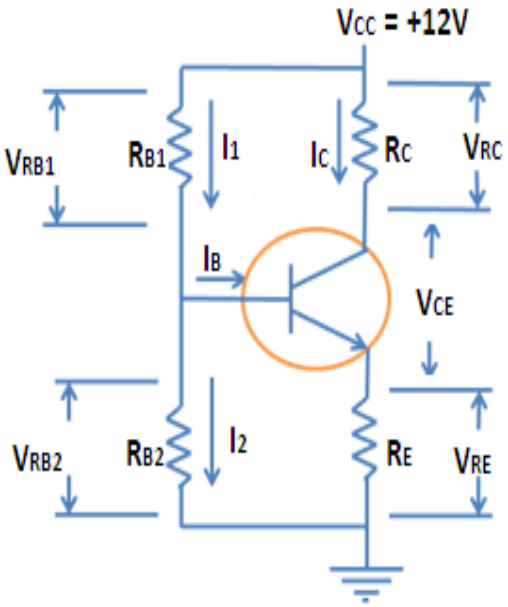
- Negative feedback can be built into the biasing circuit so that increased collector current leads to decreased base current. Hence, the increasing collector current throttles its source.
- Heat sinks can be used that carry away extra heat and prevent the base–emitter temperature from rising.
- The transistor can be biased so that its collector is normally less than half of the power supply voltage, which implies that collector–emitter power dissipation is at its maximum value. Runaway is then impossible because increasing collector current leads to a decrease in dissipated power; this notion is known as the half-voltage principle.

There are different types of biasing circuits are available. Some are given below:

- Fixed bias
- Collector to base feedback bias
- Emitter stabilized bias
- Voltage divider bias

Voltage Diver Bias Circuit:

This is a very stable bias circuit. The currents and voltages are nearly independent of any variations in β.The idea is that the voltage divider maintains a very stable voltage at the base of the transistor, and since the base current is many times smaller than the current through the divider, the base voltage remains practically unchanged.



R_{B1}=68kΩ

R_{B2}=27kΩ

R_C=3.3kΩ

R_E=1.5kΩ

Q =2N3904

The resistor RE provides the negative feedback. Due to the fact that the base voltage remains unchanged, the negative feedback works very effectively and any unwanted increment of the current gain produces an almost equal negative feedback. The collector and emitter currents change just a few, and the Q point remains practically stable. Analysis can be done in 2 methods

- Exact analysis
- Approximate analysis

Approximate Analysis:

Where $I_B << I_1$ and $I_1 \cong I_2$

$$V_B = \frac{R_{B2} V_{CC}}{R_{B1} + R_{B2}}$$

Where $\beta R_E > 10 R_{B2}$

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$

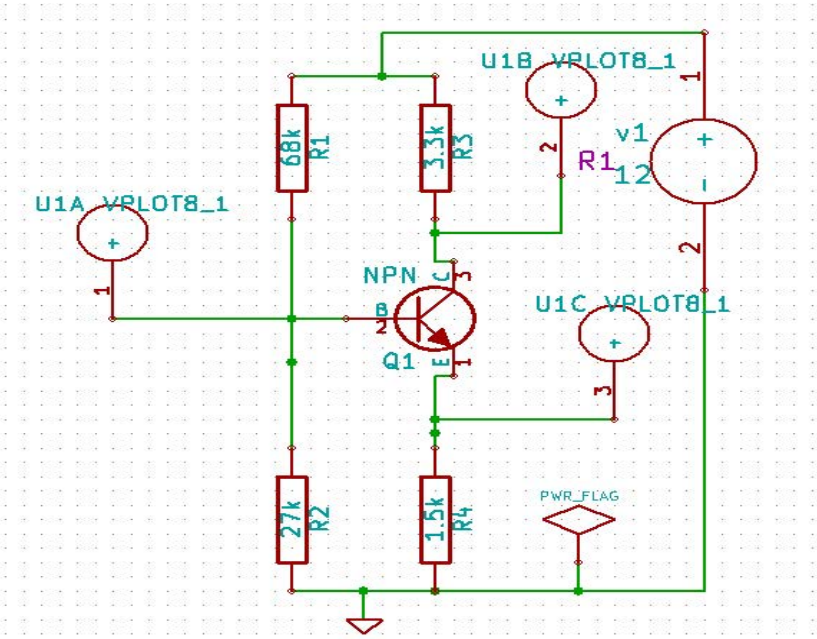
From Kirchhoff's voltage law

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

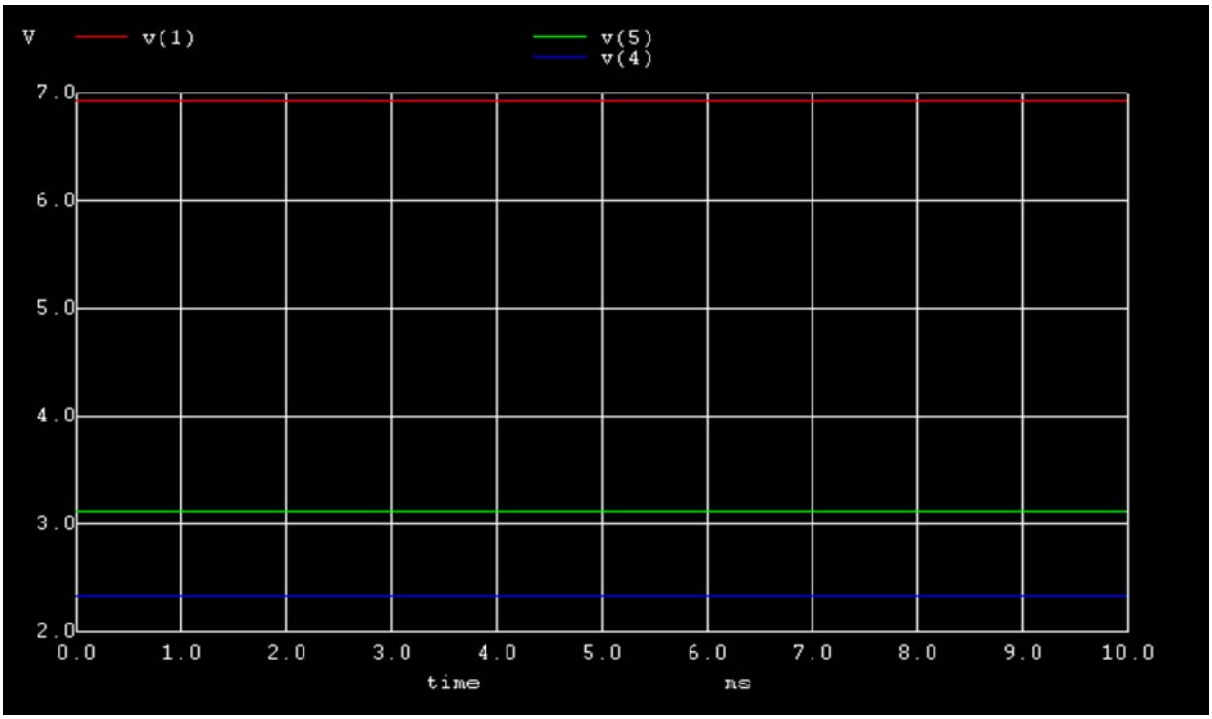
$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Schematic Circuit:



Output Waveform:



Conclusion:

Date: **Signature of the Student**

NAME:

ROLL NO.:

GROUP ID:

SUB GROUP NO.:

Experiment Mark: **/ 20** **Instructor's Signature**