EXPERIMENT NO. - 15

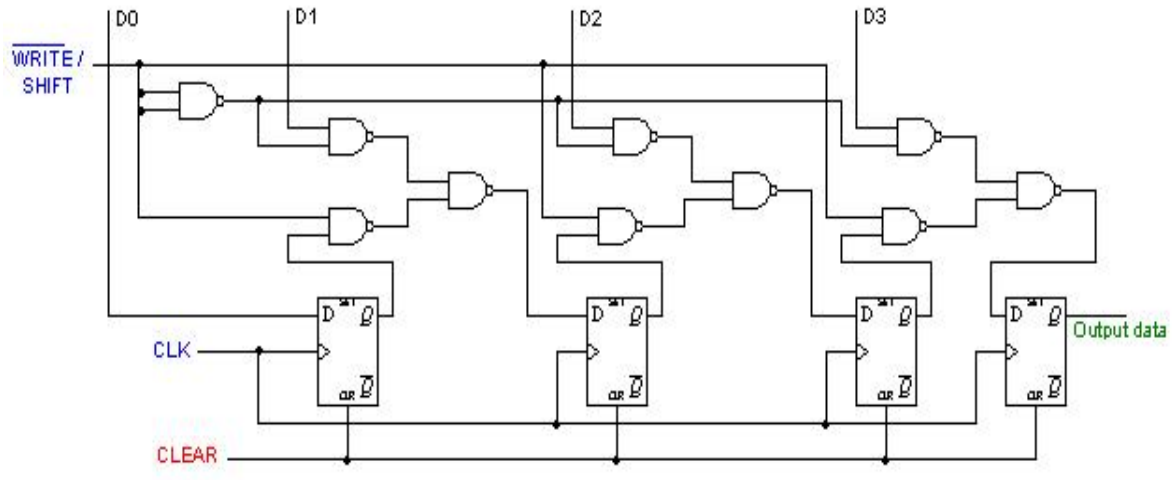
Aim of the Experiment:

Design, assemble and testing of PISO register

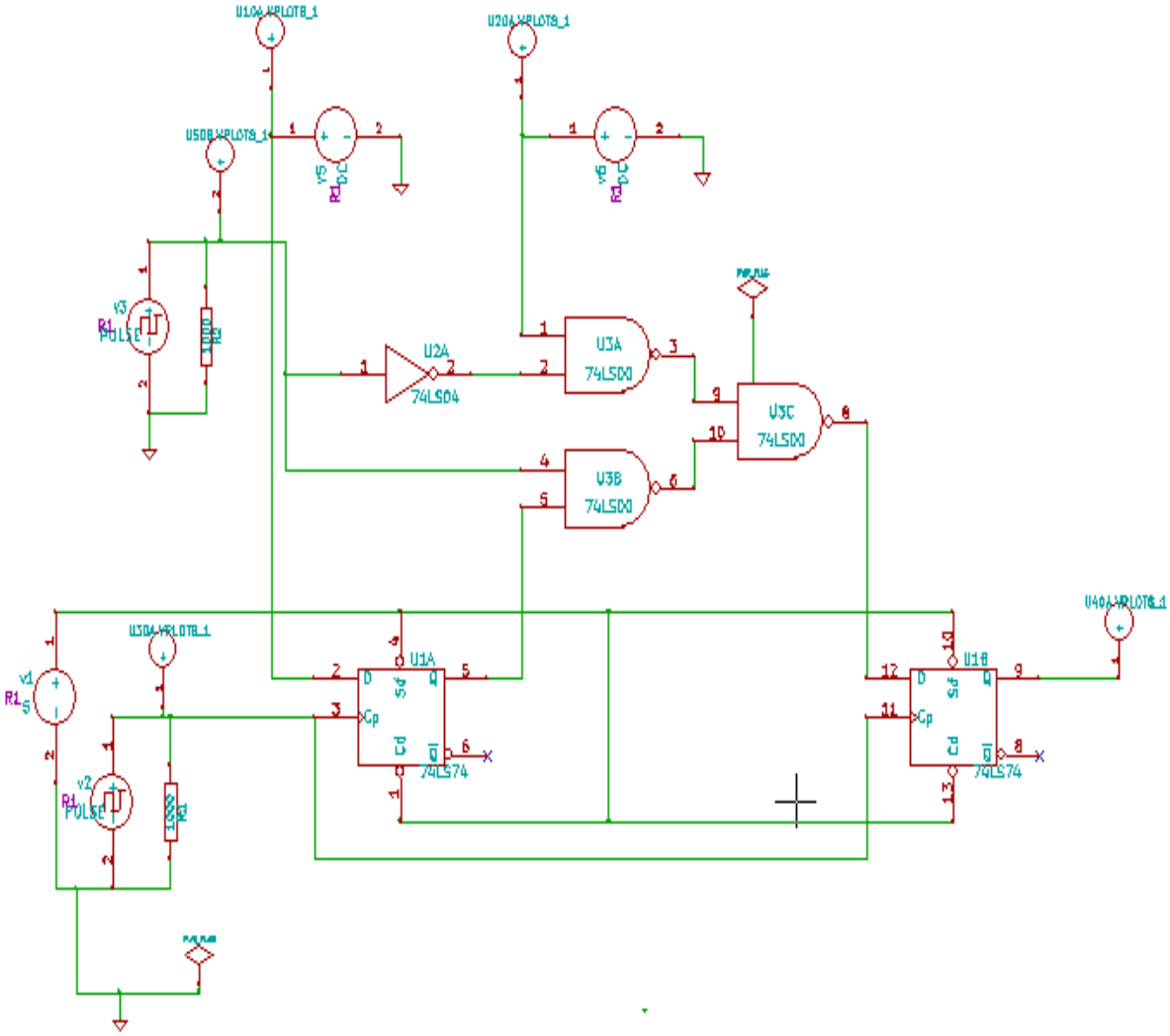
Theory:

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, *shifting in* the data present at its input and *shifting out* the last bit in the array, at each transition of the clock input.

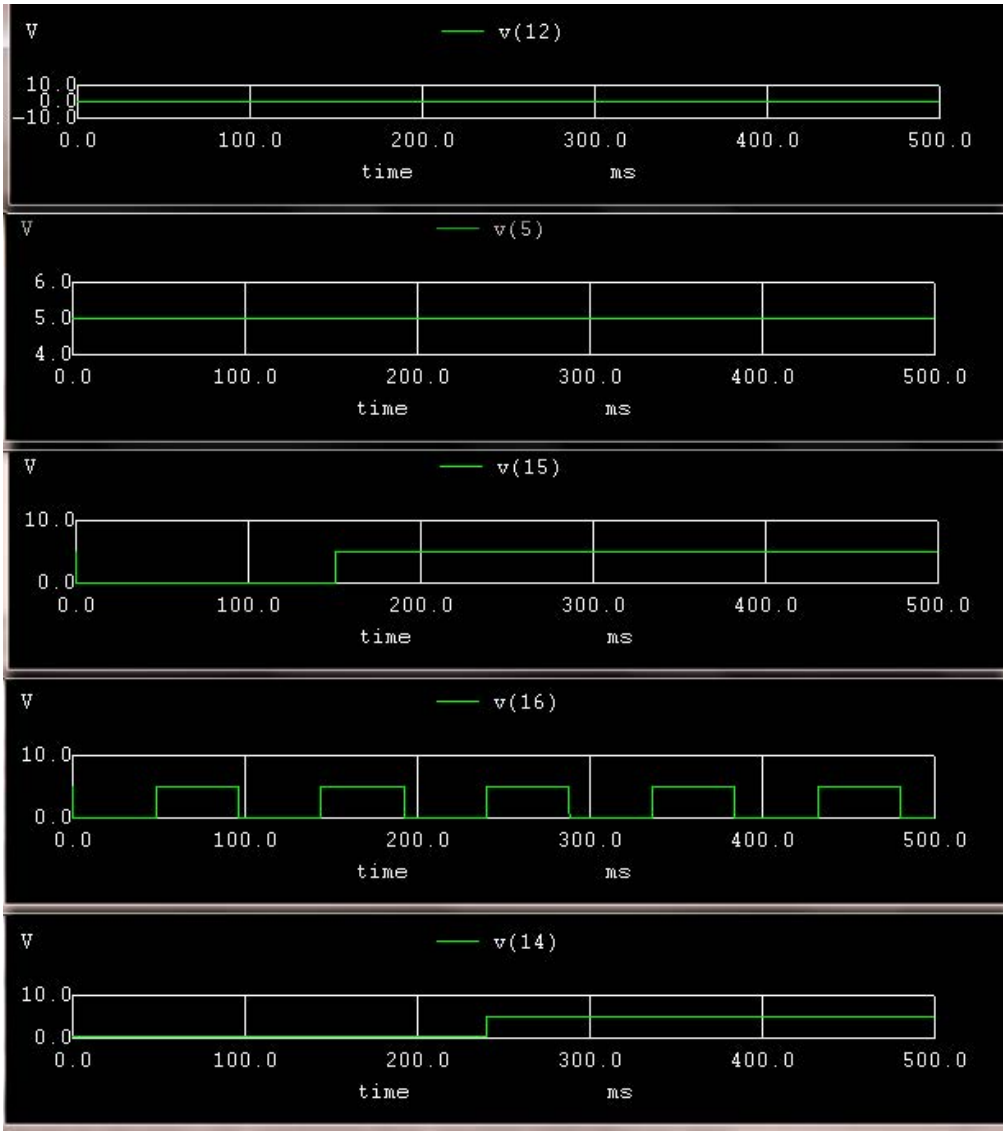
his configuration has the data input on lines D1 through D4 in parallel format, being D1 the MSB. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the W/S control line is brought HIGH and the registers are clocked. The arrangement now acts as a SISO shift register, with D1 as the Data Input. However, as long as number of clock cycles is not more than the length of the data-string, the Data Output, Q, will be the parallel data read off in order.



Schematic Circuit:



Input and Output Waveform:



1st input (LSB)

2nd input (MSB)

0-> Load
1-> Shift

Clock

Serial Output

Conclusion:

Date:

Signature of the Student

NAME:

ROLL NO.:

GROUP ID:

SUB GROUP NO.:

Experiment Mark: **/ 20** **Instructor's Signature**