# EXPERIMENT NO. - 9

## Aim of the Experiment:

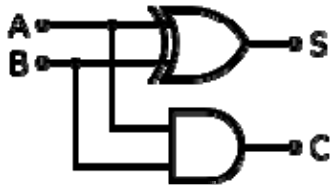
Design, assemble and testing of half adder

## Theory:

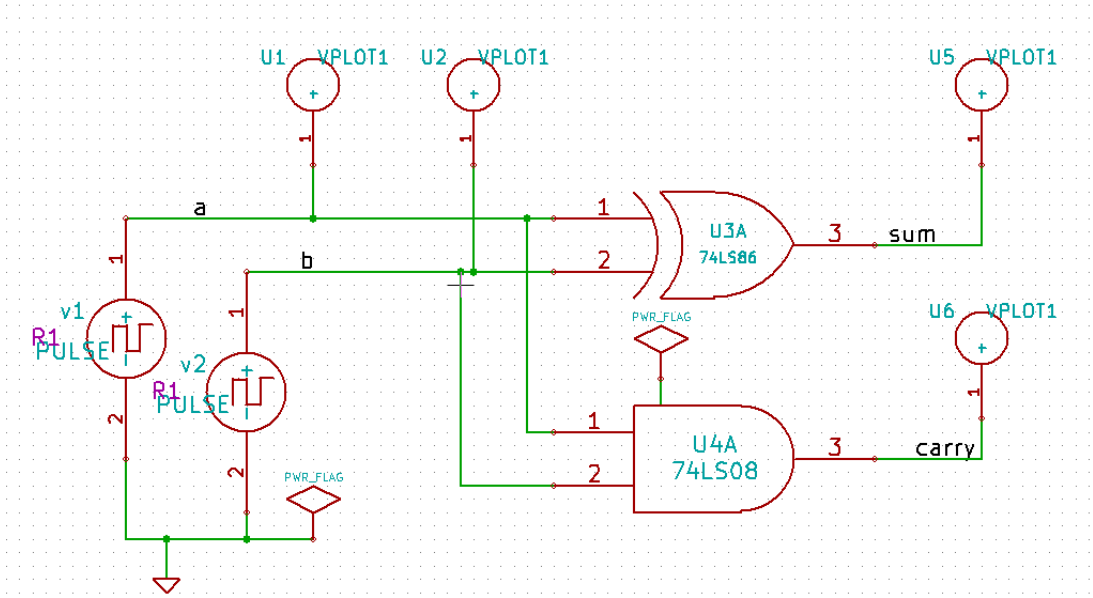
The half adder adds two single binary digits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next digit of a multi-digit addition. The simplest half-adder design, pictured on the right, incorporates an XOR gate for *S* and an AND gate for *C*. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.

The half adder adds two input bits and generates a carry and sum, which are the two outputs of a half adder. The input variables of a half adder are called the augends and addend bits. The output variables are the sum and carry. The truth table for the half adder is:

| Inputs | | Outputs | |
|---|---|---|---|
| *A* | *B* | *C* | *S* |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

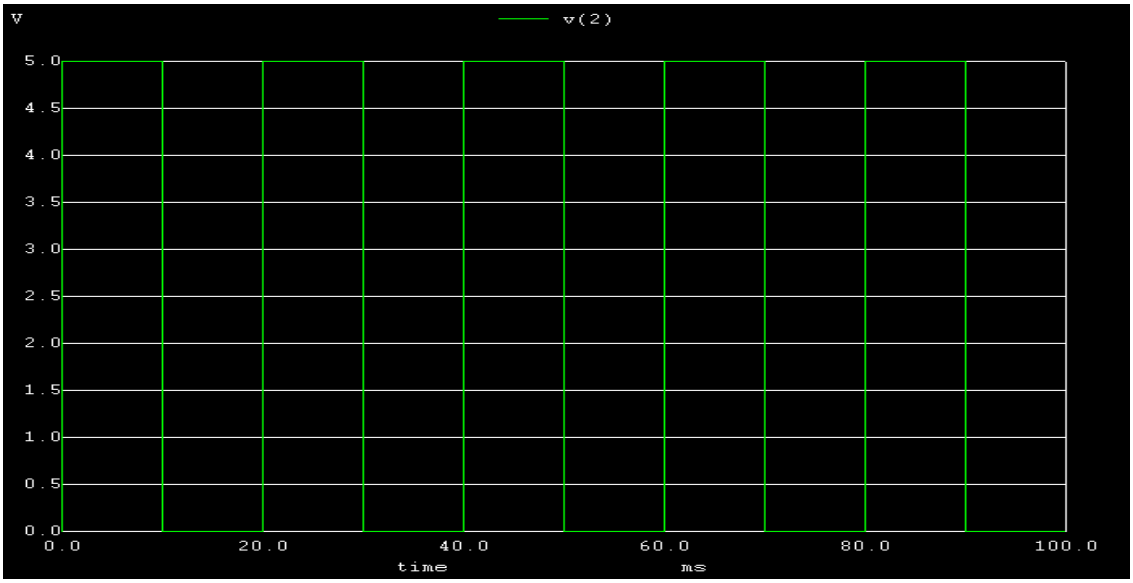


**Schematic Circuit:**

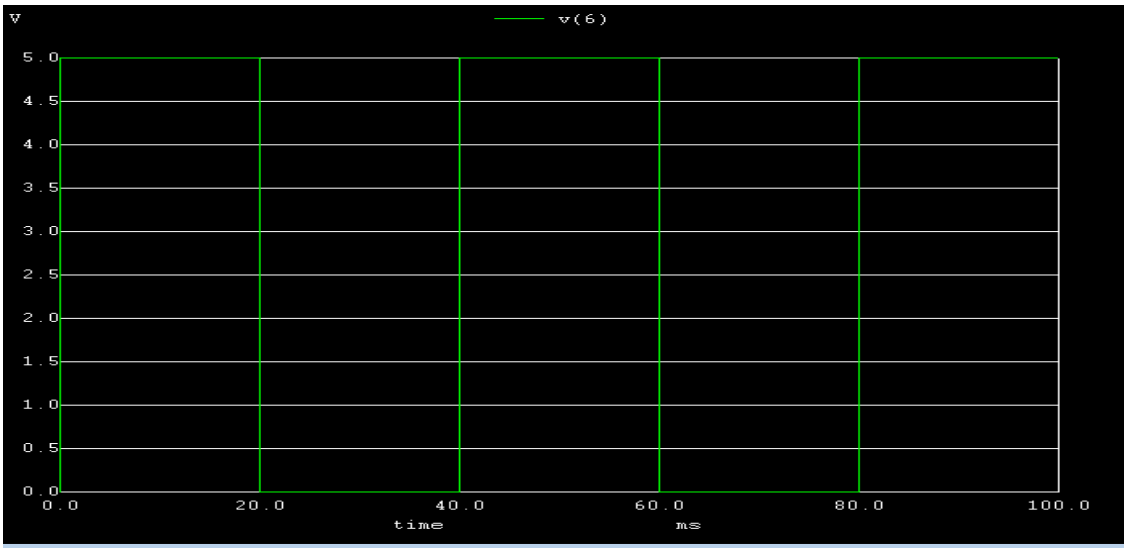



**Input Waveform:**

**a:**

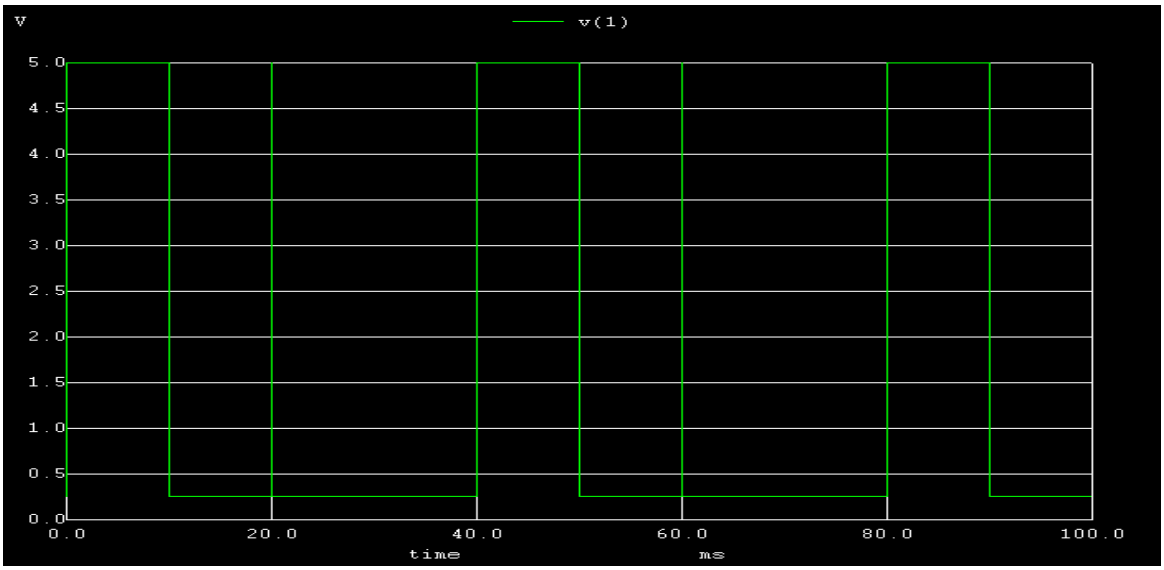


**b:**

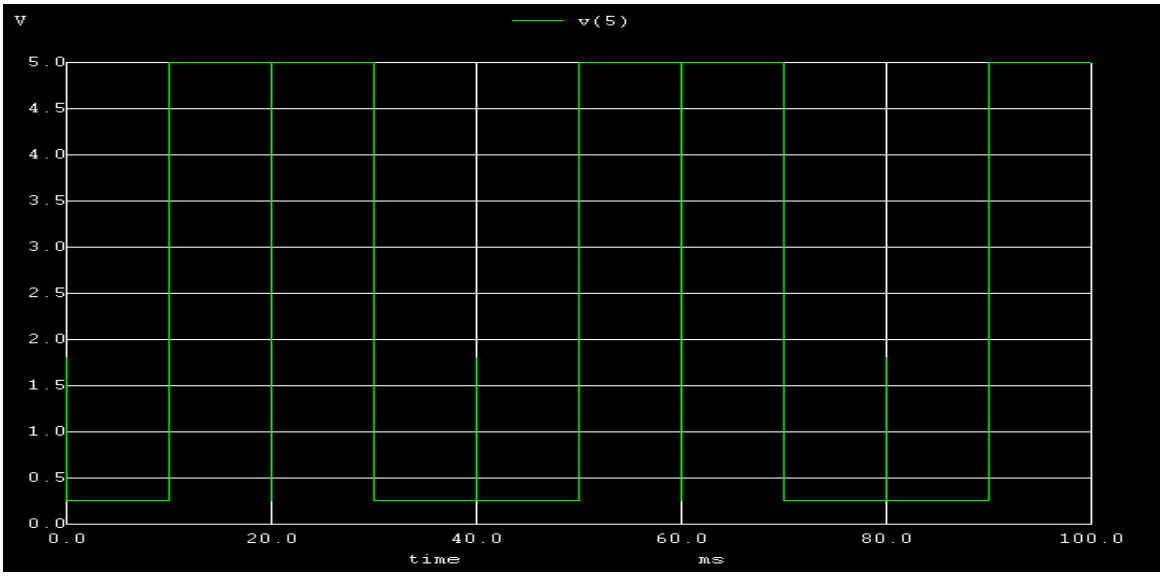



**Output Waveform:**

**Sum(S):**



**Carry(C):**




## Conclusion:

**Date**: **Signature of the Student**

**NAME:**

**ROLL NO.:**

**GROUP ID:**

**SUB GROUP NO.:**

**Experiment Mark:** **/ 20** **Instructor's Signature**