CMOS NAND GATE

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Abstract

In this, I have designed two and three-input NAND gates using skywater 130nm tech-pdk. NAND gate (NOT-AND) is a logic gate that produces an output that is false only if all its inputs are true; thus its output is a complement to that of an AND gate. Here I am using a CMOS NAND gate, It consists of two series NMOS transistors between Vout and Ground and two parallel PMOS transistors between Vout and VDD to get the desired output. The modeling includes schematics design, ngspice file to run of the above gates. Also, the simulation results of both the gates are obtained at the same node with rise time, fall time,delay.

1 Circuit Details

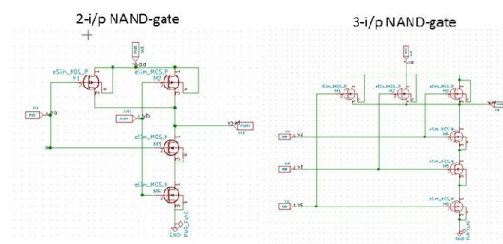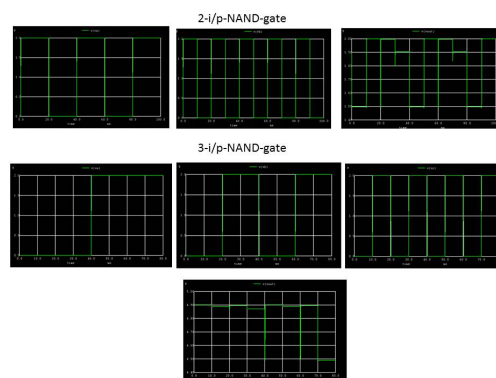This circuit diagram demonstrates the CMOS static two-input and three-input NAND gates are as shown in Figure.1. The schematic is made using eSim Schematic Editor. The two-input NAND gate uses two p-channel transistors in parallel between VCC and gate-output, and the complementary circuit of a series-connection of two n-channel transistors between GND and gate-output as shown in figure.1.(2-i/p-NAND-gate). The three-input NAND gate uses three p-channel transistors in parallel between VCC and gate-output, and the complementary circuit of a series-connection of three n-channel transistors between GND and gate-output as shown in figure.1.(3-i/p-NAND-gate). If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Vout to Ground. Hence, the output will be logic low. The n-net consisting of two series-connected NMOS transistors creates a conducting path between the output node and the ground. only if both input voltages are logic-high, i.e., are equal to VOH. In this case, both of the parallel-connected PMOS transistors in the p-net will be off. For all other input combinations, either one or both of the PMOS transistors will be turned on, while the n-net is cut-off, thus creating a current path between the output node and the power supply voltage. A switching threshold voltage of VDD/2 (for simultaneous switching).

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] M. K. J. S. U. Balraj Singh. Analysis_of_cmos_based_nand_and_nor_gates_at_45_nm_technology. https://www.researchgate.net/publication/316548029_Analysis_of_C