Dynamic charge sharing comparator

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July 23, 2021

Abstract

This dynamic charge sharing comparator has a fairly symmetric design, incorporating only MOSFETs, thus, enabling effective layout strategies to be utilised. It has been designed with a ff library from the provided options in the model and the same was decided by going through different options apart from those. The output pulse obtained is fairly uniform. The clock is being operated at 250 KHz here. There are various ways to implement the same, for one, using a Schmitt trigger and its hysteresis property. CMOS dynamic latched comparators are very attractive for many applications, such as high speed analog to digital converter, memory sense amplifiers, and data receivers. They use a positive feedback mechanism.

1 Circuit Details

The circuit has been designed using the practical power supply rating of 3.3 V, and the 1.8 V condition is also taken care of by providing inputs which are higher than and equal to 1.8 V. The only addition it required from the reference circuit is addition of a power flag, after ERC on eSim. The circuit is a CMOS transistor-based implementation and has two stages. The first stage being the dynamic charge sharing comparator, and the other one is the output buffer stage. The dynamic charge sharing comparator uses the circuit in the regenerative mode. In regenerative mode, the transistors operate in triode region here. The output buffer stage is self biasing differential amplifier which has differential inputs and does not have any slew rate limitations. An additional inverter is added to the output of the amplifier with the purpose of providing additional gain and to isolate the load capacitance from the amplifier. The MOSFET sizing was done heuristically by arriving at the appropriate size while keeping in mind the 0.13 um limit. The 21 MOSFET configuration consists of 7 input ports and 3 output ports, providing for a range of combinations to be fed into it, to get the required waveform. The same can be further explored but after a successful run was not pursued in this activity. The sizing is done uniformly same for PMOSFETs and for NMOSFETs. The aspect ratio is 6 to 1, with channel length capped at 0.5 um in the SPICE netlist.

2 Implemented Circuit

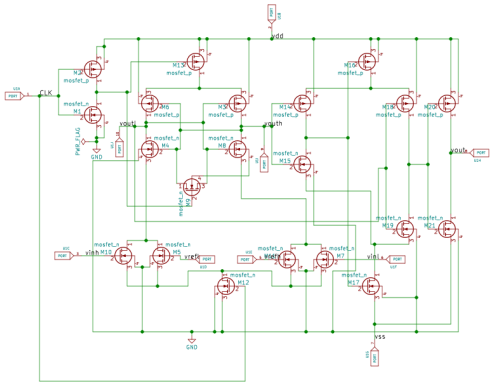

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

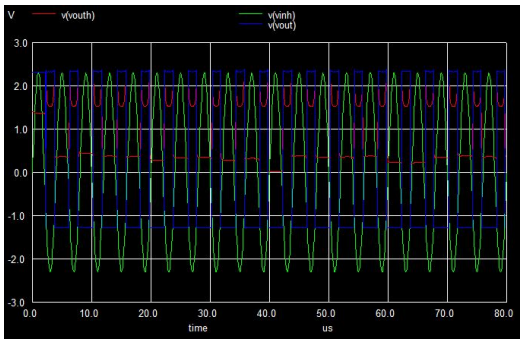

Figure 2: Implemented waveform.

References

[1] Z. Huang and P. Zhong. An adaptive analog to digital converter based on low power dynamic latch comparator. ieeexplore.ieee.org/document/1627029.

[2] D. N. Kapadia and P. P. Gandhi. Implementation of cmos charge sharing dynamic latch comparator in 130nm and 90nm technologies. ieeexplore.ieee.org/abstract/document/6558054.

[3] P. Uthaichana and E. Leelarasmee. Low power cmos dynamic latch comparators. ieeexplore.ieee.org/document/1273237.