

CMOS Used As NAND Application

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Abstract

The term CMOS stands for Complementary Metal Oxide Semiconductor. CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. CMOS offers relatively high speed low power dissipation high noise margins in both states and will operate over a wide range of source and input voltages provided the source voltage is fixed. Complementary MOS processes were widely implemented and have fundamentally replaced NMOS and bipolar processes for nearly all digital logic applications. The CMOS technology has been used for the following digital IC designs. Computer memories chip designing.

1 Circuit Details

Notice how transistors Q1 and Q3 resemble the series connected complementary pair from the inverter circuit. Both are controlled by the same input signal input A. the upper transistor turning off and the lower transistor turning on when the input is high 1 and vice versa. Notice also how transistors Q2 and Q4 are similarly controlled by the same input signal input B and how they will also exhibit the same on/off behavior for the same input logic levels. The upper transistors of both pairs Q1 and Q2 have their source and drain terminals paralleled, while the lower transistors Q3 and Q4 are series-connected. What this means is that the output will go high 1 if either top transistor saturates and will go low 0 only if both lower transistors saturate. The complementary P and N channel MOSFET pairs of a CMOS gate circuit are ideally never conducting at the same time there is little or no current drawn by the circuit from the Vdd power supply except for what current is necessary to source current to a load. CMOS gate inputs are sensitive to static electricity. They may be damaged by high voltages, and they may assume any logic level if left floating. Pullup and pulldown resistors are used to prevent a CMOS gate input from floating if being driven by a signal source capable only of sourcing or sinking current. CMOS gates are able to operate on a much wider range of power supply voltages typically 3 to 15 volts.

2 Implemented Circuit

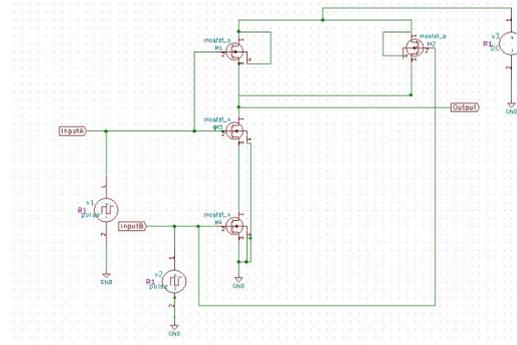


Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

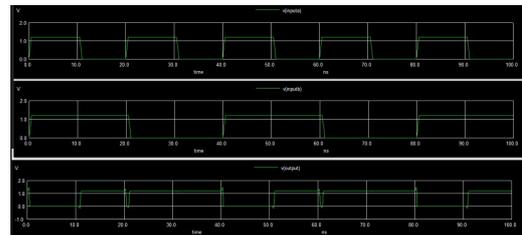


Figure 2: Implemented waveform.

References

- [1] R. Heinlein. Cmos gate circuitry. <https://www.allaboutcircuits.com/textbook/digital/chpt-3/cmos-gate-circuitry/>.
- [2] M. Sharma. Cmos working construction and applications. <http://mpithathras.in/files/2020-05-03doc37516.pdf>.