

CMOS Inverter

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Abstract

The term CMOS stands for “Complementary Metal Oxide Semiconductor”. This is one of the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. The CMOS inverter is an important circuit device that provides quick transition time, high buffer margins, and low power dissipation: all three of these are desired qualities in inverters for most circuit design. It is quite clear why this inverter has become as popular as it is.

1 Circuit Details

In CMOS technology, both N-type and P-type transistors are used to design logic functions. An equivalent signal which activates a transistor of 1 type is employed to show OFF a transistor of the opposite type. This characteristic allows the planning of logic devices using only simple switches, without the necessity for a pull-up resistor. In CMOS logic gates a set of n-type MOSFETs is arranged during a pull-down network between the output and therefore the low voltage power supply rail (V_{ss} or very often ground). rather than the load resistor of NMOS logic gates, CMOS logic gates have a set of p-type MOSFETs during a pull-up network between the output and therefore the higher voltage rail (often named V_{dd}). Thus, if both a p-type and n-type transistor have their gates connected to an equivalent input, the p-type MOSFET are going to be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such one is ON and therefore the other OFF for any input pattern. CMOS offers relatively high speed. It consists of PMOS and MOS FET. The input A is the gate voltage for both transistors. The NMOS transistor has input from V_{ss} (ground) and therefore the PMOS transistor has input from V_{dd} . The terminal Y is output. When a high voltage (V_{dd}) is given at input terminal (A) of the inverter, the PMOS becomes an circuit, and NMOS transitioned therefore the output are going to be pulled right down to V_{ss} .

2 Implemented Circuit

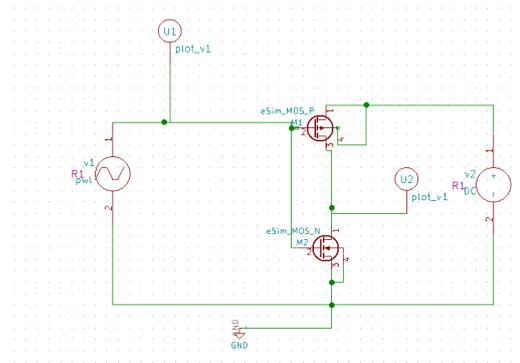


Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

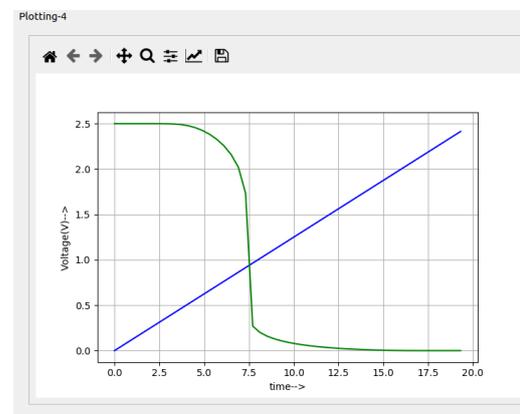


Figure 2: Implemented waveform.

References

- [1] elprocus. What is a cmos : Working principle & its applications. <https://www.elprocus.com/cmos-working-principle-and-applications/>.
- [2] N. Moore. Design, layout, and simulation of a cmos inverter. <http://cmosedu.com/jbaker/courses/ee421L/f13/students/mooren14/>
- [3] B. Sales. A simple description of the characteristics of cmos inverters. https://courseware.ee.calpoly.edu/dbraun/courses/ee307/F02/02_Sale