NOR gate using CMOS 130 technology

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Abstract

The basics logic gate is an idealized or physical device that implement a Boolean function. Logic gates have two inputs and one output and based on a Boolean function (True or False). In logic gates, true represents 1 and false represents 0. It can be thought of like a light switch, where at one position it is ON and output is (1), and at another it is off (0). And logic gates are implemented using transistor like NOR gate and etc. Logic gates uses a combination of digital signals which takes one or more than one input and gives a result as output. So, we have designed a logic circuit NOR gate using CMOS in 130nm technology. And, CMOS are very power efficient which dissipate nearly zero power in ideal state.

1 Circuit Details

We are designed a CMOS (complementary-metal-oxide-semiconductor) NOR gate circuit using a MOSFET N-channel FET (Field effect transistor) and P-channel FET (Field effect transistor). A CMOS NOR gate circuit uses a MOSFET these are two types of MOSFET one is N-MOS which are connect in parallel and any other one P-MOS are in connect series. The first P-MOS as M1 and M2 another N-MOS as M3, and M4 and also are connected VDD and GND (ground). In this esim circuit designed we are going to the 2 input NOR gate using 130nm technology. First input A and second input B which is passing into N-MOS and P-MOS and output are obtained at Y. 1) When Low (0) input in both A and B input of p-MOS and N-MOS: PMOS M1 and M2 comes in ON state and also, at a same time Both N-MOS M3 and M4 comes in OFF state. So, it gives VDD at output Y comes HIGH (1). 2) When Low (0) input is given to A and High (1) input is given to B of P-MOS and N-MOS: P-MOS M1 comes in ON state and M2 comes in OFF state. And N-MOS M3 comes in OFF state and M4 comes in ON state. So it gives GND at output Y comes LOW (0). 3) When HIGH (1) input is given to A and LOW (0) input is given to B of P-MOS and N-MOS: P-MOS M1 comes in OFF state and M2 comes in ON state. And N-MOS M3 comes in ON state and M4 comes in OFF state. So, it gives GND at output Y comes LOW (0). 4) When HIGH (1) input in both A and B input of P-MOS and N-MOS: PMOS M1 and M2 comes in OFF state and also, at a same time Both N-MOS M3 and M4 comes in ON state. So, it gives GND at output Y comes LOW (0).
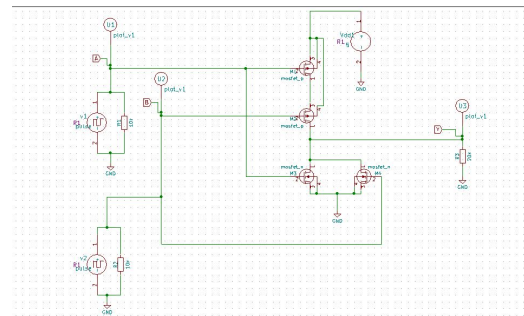
2 Implemented Circuit

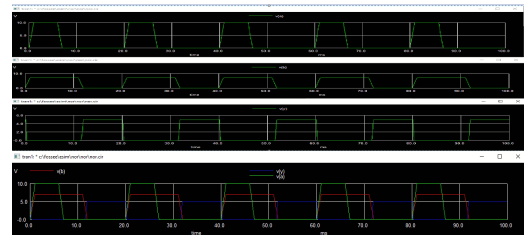Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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