DESIGN OF 3 INPUT NAND GATE USING CMOS

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Abstract

To design 3input NAND gate using CMOS to observe transient response for input pulse signals. The three input NAND gate uses three p channel transistors in parallel between vdd and drain output, and the complementary circuit of a series connection of three n channel transistors between GND and drainoutput.Unlike the 2 input NAND gate, the 3 input NAND gate has three inputs. The Boolean expression of the logic NAND gate is defined as the binary operation dot,The NAND gate can be cascaded together to form any number of individual inputs. There are 23=8 possible combinations of inputs.For the design of any circuit with the CMOS technology need parallel or series connections of NMOS and PMOS transistors.
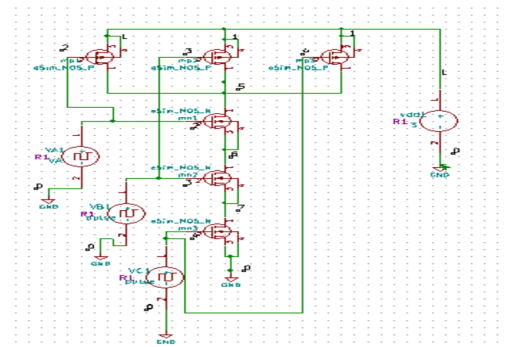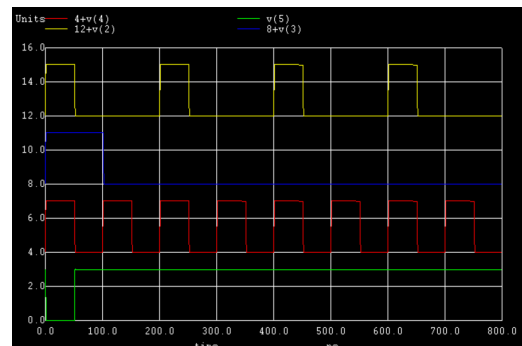
1 Circuit Details

It consists of three series NMOS transistors between output and Ground and three parallel PMOS transistors between output Y and VDD Sum terms are connected parallel and product terms are connected series so NMOS = A dot B dot C PMOS = A bar B bar C = A bar plus B bar plus C bar Y = (A dot B dot c dot) bar truth table if A=0 B=0 C=0 output=1

A=0 B=0 C=1 output=1 A=0 B=1 C=0 output=1 A=0 B=1 C=1 output=1 A=1 B=0 C=0 output=1 A=1 B=0 C=1output=1 A=1 B=1 C=0 output=1 A=1 B=1C=1 output=0

Case1 VA Low VB Low VA Low pMOS1 ON nMOS1 OFF VB Low pMOS2 ON nMOS2 OFF Path establishes from Vdd to Vout through the series connected ON pMOS transistors and Vout gets charged to Vdd level No path from Vout to GND Therefore no discharging and hence Vout will be High Case2 VA Low VB High VA Low: pMOS1 ON nMOS1 OFF VB High pMOS2 OFF nMOS2 ON In this case path establishes from Vout to GND through nMOS2 but no path to Vdd So Vout would get discharged and will be at level Low Case3 VA High VB Low VA High pMOS1 OFF nMOS1 ON VB Low pMOS2 ON nMOS2 OFF The explanation is similar as case2 Vout will be at level Low In case of NAND gate 3 pMOS will be connected in parallel and 3 nMOS will be connected in series and other way around in case of 3 input NOR gate The same pattern will continue even if for more than 3 inputs

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] J. M. Rabaey. Digital integrated circuits: A design perspective. https://booksonweb.files.wordpress.com/2011/11/digital-integrated-circuits-a-design-perspective-by-jan-m-rabaey.pdf.