CMOS 2:1 MUX Design and Implementation

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Abstract

Multiplexer (MUX) is one of the important components of communication system, to increase the efficiency of data transmission, to utilize the vast memory space of a computer in an effective way and to convert parallel form of data into serial form in telecommunication networks an efficient design of low power-delay MUX is required. MUX is a data selector with 2n input lines that selects one of several analog or digital input signals and forwards the selected input into a single output line. Multiplexer is a convenient module for the design of several dominant circuits. This paper proposes a narrative and efficient module of a CMOS based 2:1 multiplexer.

1 Circuit Details

The given 2:1 MUX has two inputs(A,B), one selection input (S), and one output line(Y). Therefore, it can have only two achievable combination, i.e. 0,1. When selection input is '0' then input line 'A' is preferred and is directed to the output, Y. Similarly, when selection input is '1' then input line 'B' is preferred and is directed to the output, Y. CMOS based 2:1 MUX is build up of two sections namely, pull up lattice and pull down lattice. Pull up lattice is known as PMOS and pull down lattice is known as NMOS. In this model, PMOS device is connected to the supply voltage (VDD) and NMOS is connected to the ground (GND). Both PMOS and NMOS substrate is given to the source terminal (given to VDD in case of PMOS and GND in case of NMOS). From the circuit, if both A and B inputs are high, then both the NMOS transistors will conduct, neither of the PMOS transistors will conduct, and a conductive path will be established between the output and VDD, bringing the output low. If both of the A and B inputs are low, then neither of the NMOS transistors will conduct, while both of the PMOS transistors will conduct, establishing a conductive path between the output and VDD, bringing the output high. If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and VDD, bringing the output high.

2 Implemented Circuit

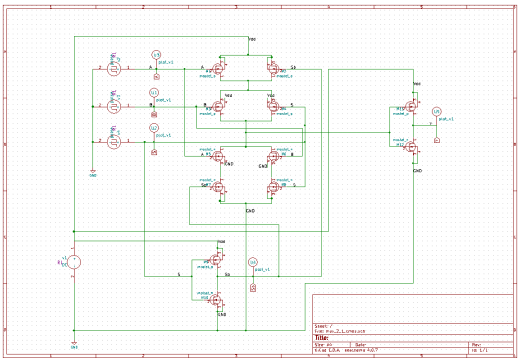

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

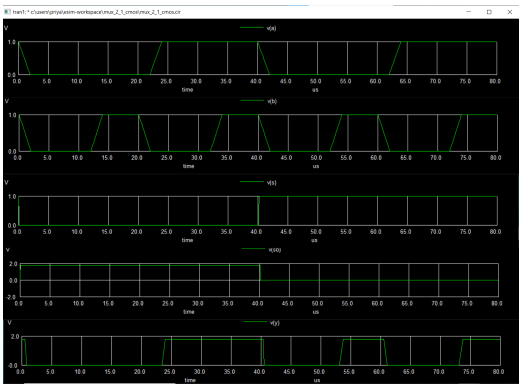

Figure 2: Implemented waveform.

References

[1] E. A. J. S. Abirami, M. Arul kumar. Design and analysis of 2:1 multiplexer circuits for high performance. http://www.arresearchpublication.com/images/shortpdf/1421139340_

[2] A. R. Tripti Dua. 2:1 multiplexer using different design style:comparative analysis. https://www.researchgate.net/publication/349211497_21_Multiplexer