Design and Analysis of Dickson Charge Pump using CMOS technology

Charaan S, Madras Institute of Technology Campus Anna University

July 7, 2021

Abstract

The Dickson Charge Pump is a DC-DC converter that produces a higher voltage than the supply voltage. Unlike the boost switching DC-DC converters which require large inductors, the Dickson Charge pump is designed using MOSFETs as switches, and they utilize energy-transfer capacitors instead of inductors, therefore the size, non-linearity, and interference issues related to the usage of inductors in ICs are being eliminated. This circuit is widely implemented in various IC applications especially in non-volatile memories like the Flash and EEPROM. In this paper, the design and analysis of a four-stage Dickson Charge Pump using the 130nm CMOS process are being discussed.

1 Circuit Details

The Dickson Charge Pump consists of the pumping capacitors which are arranged in a parallel fashion, which reduces the output impedance and increases the voltage gain as the number of stages increases. A diode-connected NMOS transistor is used for the construction of this CP. Here Vdd is the power supply voltage, NMOS transistor acts as switches, and V1 is the node voltage at the upper plate of the capacitor. Two clock sources Clk1 and Clk2 which have the same peak voltage, complementary phase, and are non-overlapping are applied to each stage in an alternative manner. When Clk1 is low, Clk2 will be high due to the complementary phase and subsequently, the switch MD1 is turned ON and the first capacitor is charged by the voltage source Vdd to the maximum voltage of Vdd - Vt at node V1. In the next half clock, MD1 turns OFF, and the voltage Vdd provided by the Clk1, gets added to the voltage Vdd - Vt which is already present, and as a result, the voltage at node V2 becomes 2Vdd - Vt. At the same period, the switch MD2 becomes ON and the next capacitor is charged through MD2 by the voltage 2Vdd- Vt, to a maximum voltage of 2Vdd - 2Vt. In this way, the charge gets pumped from one stage to another and the node voltages at pumping capacitors of higher stages increase continuously. The final capacitor doesn't add any voltage as it is grounded and it smoothens the output. The transient analysis performed to the circuit for a Vdd of 1.8V gave an output between 4.1-4.2V for 7.5us and saturated at 4.8V for a 130nm CMOS process, and the simulation was done using eSim and SKY130 PDK.

2 Implemented Circuit

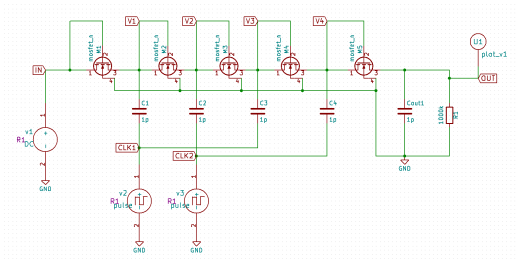

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

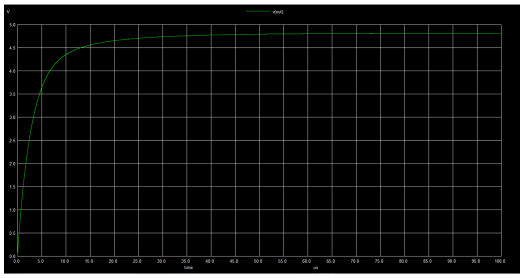

Figure 2: Implemented waveform.

References

[1] K. P. K. K. S. R. Ghosh. Dynamic gate and substrate control charge pump circuits: a review. https://www.researchgate.net/publication/275247649_Dynamic_gate_

[2] H. D. V. M. K. V. S. Jaiswal. Design and analysis of different type of charge pump using cmos technology. https://ieeexplore.ieee.org/document/7732062.

[3] A. E. A. M. F. F. E. K. K. Q. H. A. A. E. A. R. Lakhassassi. Analysis and design of dickson charge pump for eeprom in 180nm cmos technology. https://ieeexplore.ieee.org/document/8354067.