Design of 12 bit Carry Select Adder using CMOS Logic

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Abstract

Adders are the basic building blocks of advanced digital processors which process millions of instructions per second. Carry Look Ahead Adder (CLAA) logic is one of the techniques used to reduce the carry propagation delay by generating the sum and carry by considering the previous input bit conditions. In this work, a 12-bit Adder is designed using three 4 bit Carry Look Ahead Adder (CLAA) cells in cascade. The basic CLAA cell is implemented using CMOS logic. The designed 12-bit adder circuit using 4-bit CLAA as the basic cell is working properly for the input pulse signals in the 250KHz range in 1.3V supply voltage using SkyWater 130nm PDK Technology file in eSIM EDA tool.

1 Circuit Details

Over the years, several adder circuits are designed to reduce the carry propagation delay dependency. Carry Look Ahead Adders (CLAA) is one of the widely used techniques [1]. The single bit adder elements have sum(S) and carry-out (Cout) as the output in each stage [2]. Modern VLSI design prefers the modular cell structure rather than designing of individual circuits. Using these cell structures, a large number of adders are created by cascading. Higher bit adders are constructed from the basic cells. In this work, a 4-bit adder basic cell is implemented using the CLAA logic. Standard expressions are used to implement the 4-bit CLAA logic [3]. In this work, a 12-bit adder is constructed using three 4-bit CLAA cells connecting in cascade as shown in figure. Basic 4-bit adder cell is implemented in CMOS logic using the above equations. It requires 97 NMOS and 97 PMOS transistors to implement a single 4-bit CLAA cell. Simulations are carried out using the eSim EDA tool. SkyWater 130nm PDK Technology file is used in the simulations. Input pulse signals of 250 KHz and 125KHzas the digital input bits are used to check the response of the designed system. The responses of S0 to S15 and Cout show the desired results. There have been observed spikes in the simulations of the output signals when one input bit transit from 1 to 0 while the other bit from 0 to 1. If input pulses in the range of 200 MHz, the output waveforms showed the peak to peak output voltage of less than 0.5V.

2 Implemented Circuit

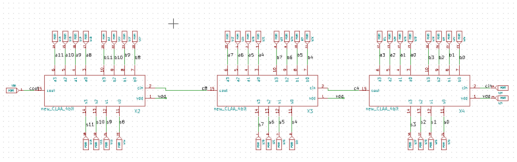

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

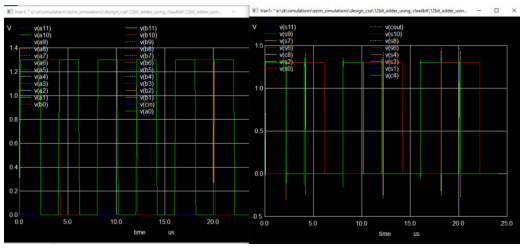

Figure 2: Implemented waveform.

References

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