Symmetric CMOS NOR Gate

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Abstract

In this paper a new CMOS n-input NOR gate is pro posed, having n parallel NMOS pull-downs to ground and n parallel PMOS pull-ups to Vcc. This new CMOS NOR gate structure is approximately twice as fast as the traditional CMOS NOR gate and is slightly faster than a CMOS inverter. The traditional CMOS NOR gate is quite slow, due to the series connection of PMOS pull-ups which has lower-mobility resistance than NMOS pull-downs, so the NOR gate encompasses a poor propagation delay. This paper proposes a new NOR gate structure that achieves higher speeds by eliminating the series connection of transistors.

1 Circuit Details

A new type of NOR gate, symmetric to PMOS and NMOS connections. This gate contains n parallel PMOS pull-ups and n parallel NMOS pull-downs. In this design of symmetric CMOS NOR gate, many CMOS inverters gang up together to form NOR gate. The PMOS is turned on when the input is low whereas the NMOS is turned on when the input is high. In the NOR gate if any one of the inputs is high then the output will be low. Consider a three-input symmetric CMOS NOR gate. when all the inputs are high then PMOS is off and NMOS turned on so that the output is low. when input A is low and the other 2 inputs are high then the output is low. when input A and C are high and B is low then the output is low. when input A, B are low and C is high then the output is low. when input A, B are high and c is low then the output is low. when the input B is high and the other 2 inputs are low then also the output is low. when input A is high and the other 2 inputs are low then the output of the NOR gate is again zero. when all the inputs are low then the output of the CMOS NOR gate is high. This is how NOR gate works. Thus the symmetric CMOS NOR gate can be faster than the traditional CMOS NOR gate so this symmetric CMOS NOR gate is used for high-speed applications. A novel feature of the symmetric circuit topology is its ability to also function as a NAND gate, merely by adjusting transistor dimensions.

2 Implemented Circuit

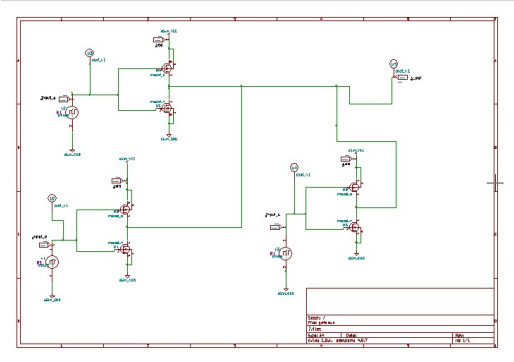

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

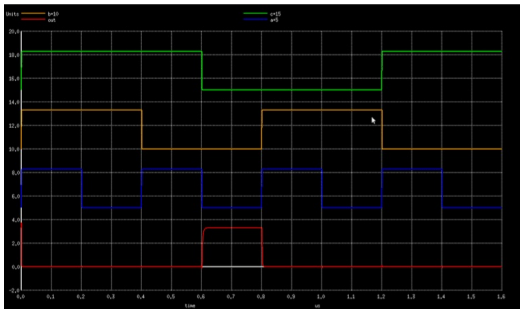

Figure 2: Implemented waveform.

References

[1] M.G.Johnson. A symmetric cmos nor gate for high speed applications. https://ieeexplore.ieee.org/document/5949.