4 bit Binary to gray code converter using 2x1 MUX

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July 1, 2021

Abstract

Low power consuming devices are playing a dominant role in VLSI design technology .The binary to gray code converter can be implemented using conventional CMOS or dual pass transistor logic or 2X1 MUX. Among these different techniques implementing using 2X1 MUX is best because it uses less power and transistors. The gray code is often used because one bit in the numerical representation changes between successive numbers. The logic is implemented using 2x1 MUX which has two inputs and one output for each multiplexer with a select line . The output is generated depending on the selection line only. These MUX are designed using pass transistor logic that uses parallel PMOS and NMOS transistors.

1 Circuit Details

The basic building blocks of binary to gray code converter is XOR gates. The XOR gate is realized using 2x1 multiplexers.. .2X1 MUX Sub circuit has PMOS and NMOS connected in parallel through the gate terminal which is select line of MUX. Two inputs of MUX is given to source of each MOSFET and drain of both MOSFET are connected to get the output. The MUX component consists of four port 2 inputs and one select line and output . The four MUX components are used in main circuit to build four bit binary code to gray code. For the first MUX the input is P and Pbar with B as select line .Pbar is obtained using inverter circuit .Depending upon B the output G0 is obtained. For the second MUX the input is C and Cbar with B as select line .Cbar is obtained using inverter circuit .Depending upon B the output G1 is obtained. For the third MUX the input is C and Cbar with D as select line .Depending upon D the output G2 is obtained. For the fourth MUX the input is D with D as select line .Depending upon D the output G3 is obtained. The inverter is obtained using CMOS. In inverter circuit the gate of PMOS and NMOS are connected together to provide the input and drain is connected together to obtain the output ,source and bulk of PMOS is connected to power source and source and bulk of NMOS is connected to ground.

2 Implemented Circuit

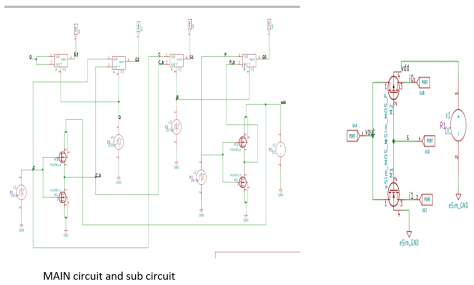

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

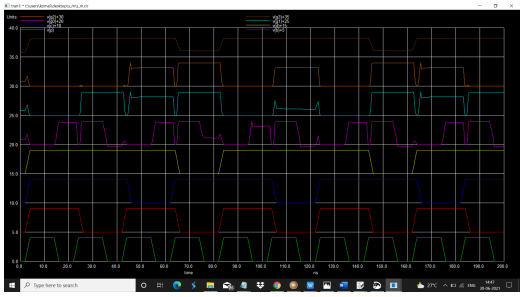

Figure 2: Implemented waveform.

References

[1] G. Sujatha and D. N. Balaji. Design and implementation of combinational circuits in different low power logic styles. http://www.iosrjournals.org/iosrjvlsi/papers/vol5-issue6/Version- 2/A05620105.pdf.