ONE BIT MIRROR ADDER WITH SKY130nm PDK & eSim tool

Shalini Kanna, University of Massachusetts Lowell

June 29, 2021

Abstract

This paper contains detailed description of a 1-Bit mirror adder advantaged and design using NMOS and PMOS. The tool used to implement this design is eSim and the models used for designing circuit are SKY130nm technology. Skywater PDK – it is an Open-source Process Design Kit with 130nm technology. For implementing this design only nfet and pfet were used with specific width and length. eSim – it is an Open-source EDA tool for circuit design, simulation, analysis and PCB design. ngSpice - It is an Open-source SPICE simulation tool. eSim had an inbuilt ngSpice simulator. Keywords – Mirror adder, Sky130, eSim, ngSpice.

1 Circuit Details

One bit Mirror adder adds up three binary inputs – A, B, Cin and produce 2 binary outputs – Sum and Carry out. Mirror adder does not have complementary pull-up and pull-down circuit. Instead, it has symmetric mirroring circuit. which means, the same circuitry is found for both NMOS logic and PMOS logic. The circuit that needs to be implement a one-bit mirror adder is shown in Fig1. The design implemented gives us Sum and Cout and the equations are obtained from normal one-bit full adder sum and carry out equations. If you see 1-Bit mirror adder you might not see much difference in processing time but if you construct multi-bit mirror adder, the advantages mentioned below can be observed especially in Carry ripple adder. Advantages: 1. In carry ripple operation, the critical path is from Cin propagated till Cout so Carry will be computed fast in mirror adder which will help in fast up the multi bit carry ripple adder. 2. A smaller number of transistors were used to implement logic i.e., 28 transistors. 3. We do not need inverted inputs. 4. It will have a uniform layout.

For simulating the spice generated from the eSim, ngSpice is used. The inputs in the spice were added in such a way that 8 combinations of the inputs can be verified. To get the proper output I have same width and length ratio for all NMOS and PMOS.

2 Implemented Circuit

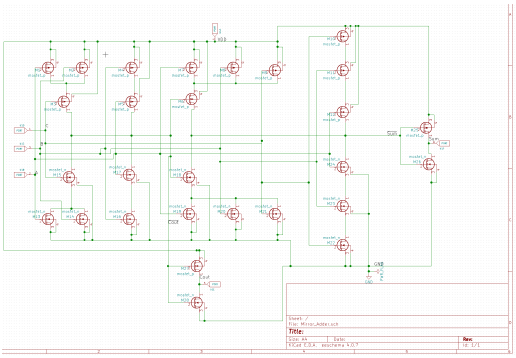

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

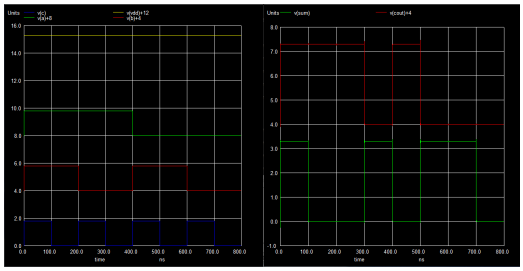

Figure 2: Implemented waveform.

References

[1] D. Harris and I. . N. Weste. "cmos vlsi design." ed: Pearson education, inc (2010). http://pages.hmc.edu/harris/cmosvlsi/4e/index.html.