Design and Analysis of Two Input NOR Gate

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Abstract

This proposed abstract constitutes of the designing and analysis of Two input NOR gate. NOR gate is the logic gate and also called as the universal gate. It is used to construct the basic gates and also Used in combinational circuits like adder, MUX etc. and in sequential circuits like flipflops and other elements. Hence, it can be considered as the key component in the designing of digital systems. The NOR gate circuit is implemented using CMOS (Complementary Metal Oxide Semiconductor) which considered to be having more power and speed. CMOS is one of the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits and in different applications.

1 Circuit Details

The Two input NOR gate CMOS (Complementary Metal Oxide Semiconductor) implementation consist of NMOS and PMOS. NMOS is constructed with the n-type source and drain and a p-type substrate, while PMOS is constructed with the p-type source and drain and an n-type substrate. In an NMOS, carriers are electrons, while in a PMOS carriers are holes. For the design of any circuit with CMOS technology, we need parallel or series connections of NMOS and PMOS. It consists of two NMOS transistors and two PMOS transistors. The two NMOS transistors are connected in a parallel patterns and the two PMOS transistors are connected in the series pattern. Two series (upper) transistors connected to Vdd and two parallel-connected (lower) transistors connected to the ground. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low. It has two inputs and one output. In these two PMOS connected in series and it is a pull-up network now this is connected to pull down network by using NMOS in parallel connection. The output is taken between pullup and pulldown network. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low. The NOR gate output is HIGH (1) if both the inputs to the gate are LOW (0) and if one or both input is HIGH (1) then a LOW (0) output results.

2 Implemented Circuit

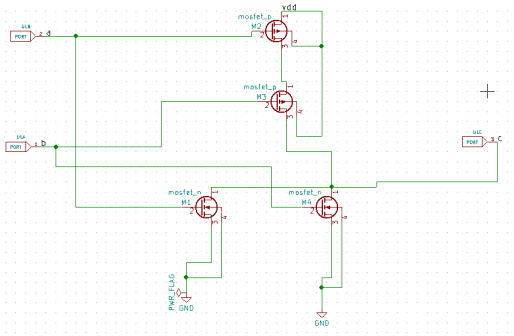

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

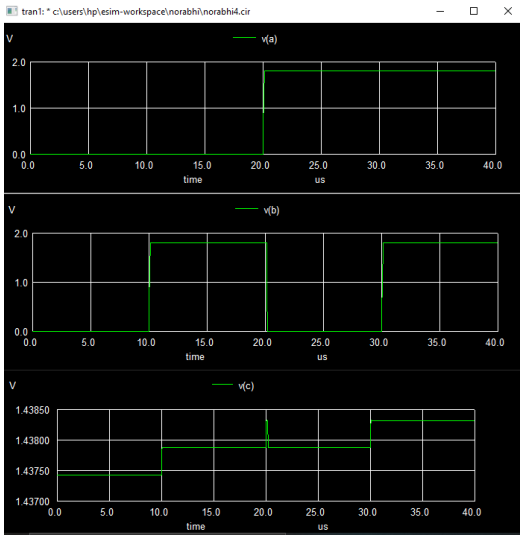

Figure 2: Implemented waveform.

References

[1] F. Aloul and A. S. B. A. Rawi. Exciting stuck-open faults in cmos circuits using ilp techniques. https://ieeexplore.ieee.org/abstract/document/1618388.

[2] A. Singhal. Universal logic gates | nand gate | nor gate. https://www.gatevidyalay.com/universal-gates/.