A Conventional 2 input CMOS NAND gate circuit

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Abstract

NAND gate is one of the basic building blocks of digital Circuits . It is the combination of AND Gate followed by NOT gate it is the complementary of AND gate. Key to this gate circuit s elegant design is the complementary use of both P and N channel IGFETs. Since IGFETs are more commonly known as MOSFETs Metal Oxide Semiconductor Field Effect Transistor and this circuit uses both P and N channel transistors together the general classification given to gate circuits like this one is CMOS Complementary Metal Oxide Semiconductor. The truth table shows all the possible operation of NAND gate using CMOS

1 Circuit Details

CMOS is the combination of PMOS and NMOS. The circuit shows the realization of CMOS NAND gate which consists of two PMOS and two NMOS gates. Transistors M1 and M3 resemble the series connected complementary pair from the inverter circuit . Both are controlled by the same input signal input 1 the upper transistor turning off and the lower transistor turning on when the input is high 1 and vice versa . Transistors M4 and M2 are similarly controlled by the same input signal input 2 and they will also exhibit the same on/off behavior for the same input logic levels . The upper transistors of both pairs M1 and M4 have their source and drain terminals paralleled, while the lower transistors M3 and M2 are series connected . This means that the output will go high 1 if either top transistor saturates, and will go low 0 only if both lower transistors saturate . If both the inputs 1 and 2 are HIGH inputs, which make the MOSFETs M3 M2 to be turned ON and M1, M4 to be turned OFF . Field-effect transistors particularly the insulated-gate variety are used in the design of gate circuits. Being voltage controlled rather than current-controlled devices, IGFETs tend to allow very simple circuit designs . Pulsated input is provided at inputa, inputb , vdd for dc and output is obtained . The Circuit diagram for the 2 input CMOS NAND Gate is shown in the figure with the obtained waveform for reference

2 Implemented Circuit

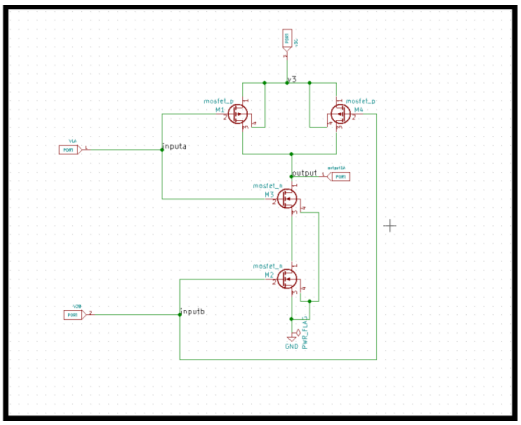

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

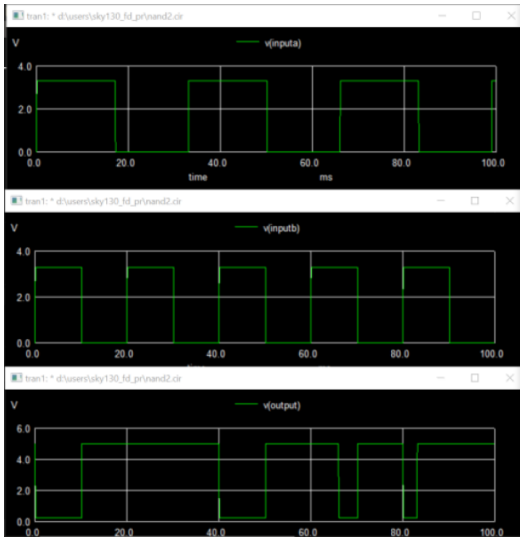

Figure 2: Implemented waveform.

References

[1] J. . A.N. Variable input delay cmos logic for d latch circuit'. https://www.researchgate.net/publication/304132213_Variable_Input_

[2] M. . J. B. . Ragini, K. & Satyam. Variable threshold mosfet approach (through dynamic threshold mosfet) for universal logic gates. https://www.researchgate.net/publication/220480907_Variable_Thres