CMOS Schmitt Trigger

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Abstract

Schmitt trigger is a comparator circuit with positive feedback that accepts an oscillating signal and outputs a square wave. It is a bistable circuit whose output switches between two steady state voltage levels either high or low. When the output is high and the input exceeds the upper threshold, the output switches low and if the output is low and the input falls below the lower threshold, the output switches high again. This dual-threshold action is called hysteresis and with this unique property, the circuit can be utilized for the detection of low to high and high to low switching events in noisy environments. If a noisy signal is given as an input to a Schmitt trigger the output will be a clean signal.

1 Circuit Details

The input of the Schmitt trigger is tied to the gates of four CMOS devices. The upper two are PMOS and the lower two are NMOS. Transistors M6 and M3 act as source followers and introduce hysteresis by feeding back the output voltage. The Schmitt trigger circuit can be divided into two parts depending on whether the output is high or low. When the output is low and the input is high the transistors M5 and M4 are OFF and M6 is ON. As M6 is ON it creates an additional path to the ground for node X. When Vin makes the transition from Vdd to 0, transistors M5 and M6 will turn ON. But some current charging output will be diverted through this node X to the ground until the output goes high and turns OFF M6.So Vin has to go much lower for the transition. Similarly, When the output is high and the input is low the transistors M1 and M2 are OFF and M3 is ON. So when M3 is ON there will be a path to the Vdd for the node Y. When Vin makes the transition from 0 to Vdd, transistors M1 and M2 will turn ON and will try to pull the Vout to the ground but before that, it has to sink the additional current from Vdd, until the output goes low and turns OFF M3. Hence, Vin has to go much higher to make the output low. The upper and lower threshold voltages of the Schmitt trigger are set by choosing appropriate W and L of PMOS & NMOS transistors.
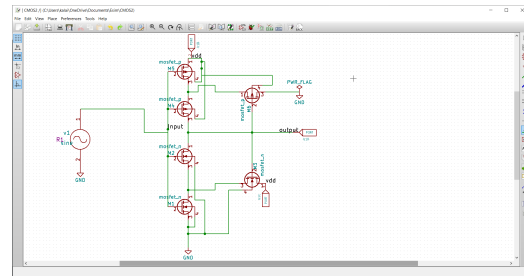
2 Implemented Circuit

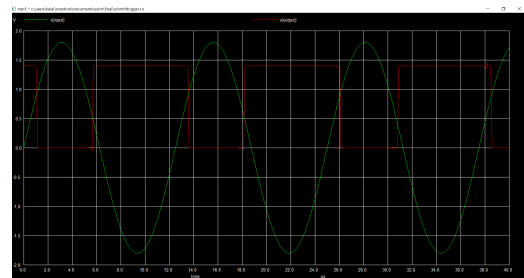Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] R. Baker. Cmos:circuit design,layout,andsimulation. https://www.researchgate.net/publication/295256070CMOSCircuitDe