

# Circuit Simulation Project

<https://esim.fossee.in/circuit-simulation-project>

**Name of Participant:** Navin Kumar M

**Project Guide:** Dr. Maheswari. R

## **Title of the Project: -**

**Design of a 4-Bit Binary Combinational Lock using  
Subcircuit Builder in eSIM**

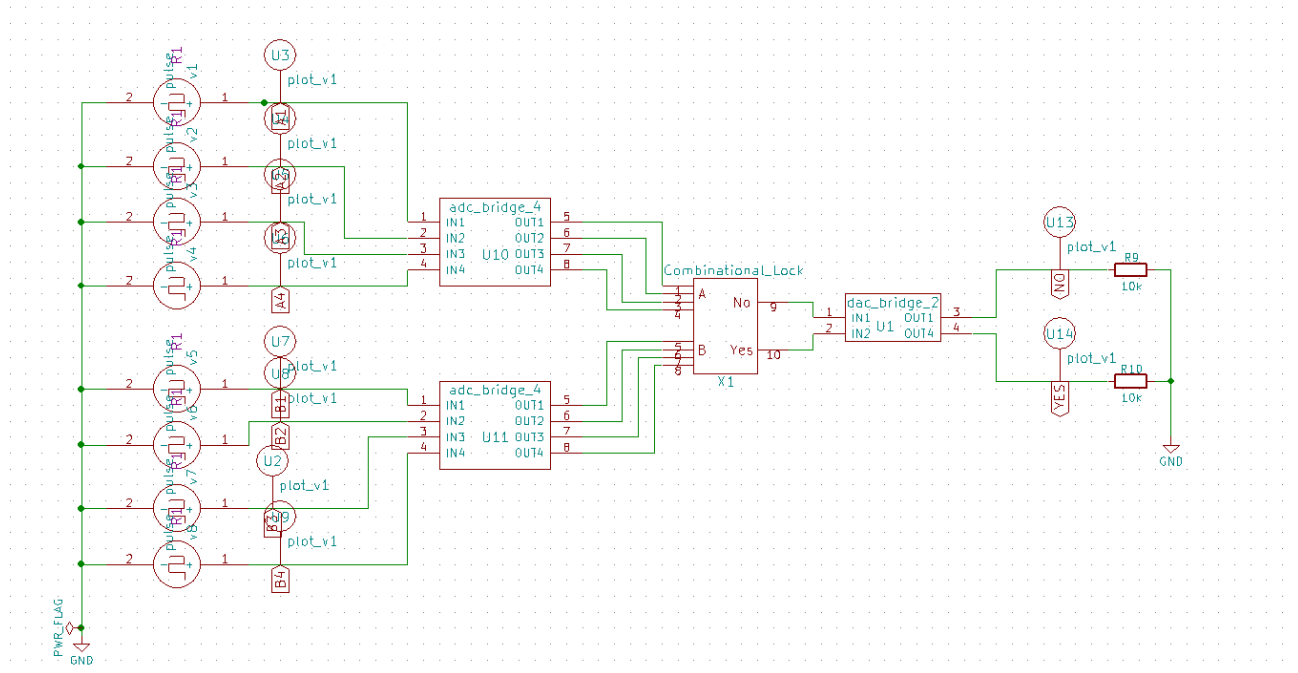
## **Theory/Description: -**

Combinational locks are generally used in preventing crime and intrusion prevention. These usually require the user to enter a numerical sequence to gain entry. The 4 – bit binary combinational lock is designed and constructed using simple circuit elements and is implemented with digital electronic logic gates such as D-NOR, D-XOR and Diodes. ADC and DAC are used to convert analog signals to digital signals and digital signals to analog signals respectively. Here, we created combinational lock sub circuit which is used as a component in the main circuit.

In the main circuit, 8 – pulse generators are used where each one represents a binary digit. High voltage is Ob1 and low voltage is Ob0. First four pulse generators represent 4- bit binary combination which is set by the user as password and the remaining four pulse generators are the passcode combination which the user enters to unlock the lock. If the password that is set originally matches with the password entered by the user, then YES flag will be outputted with high voltage (Ob1). Else, NO flag will be outputted with low voltage (Ob0).

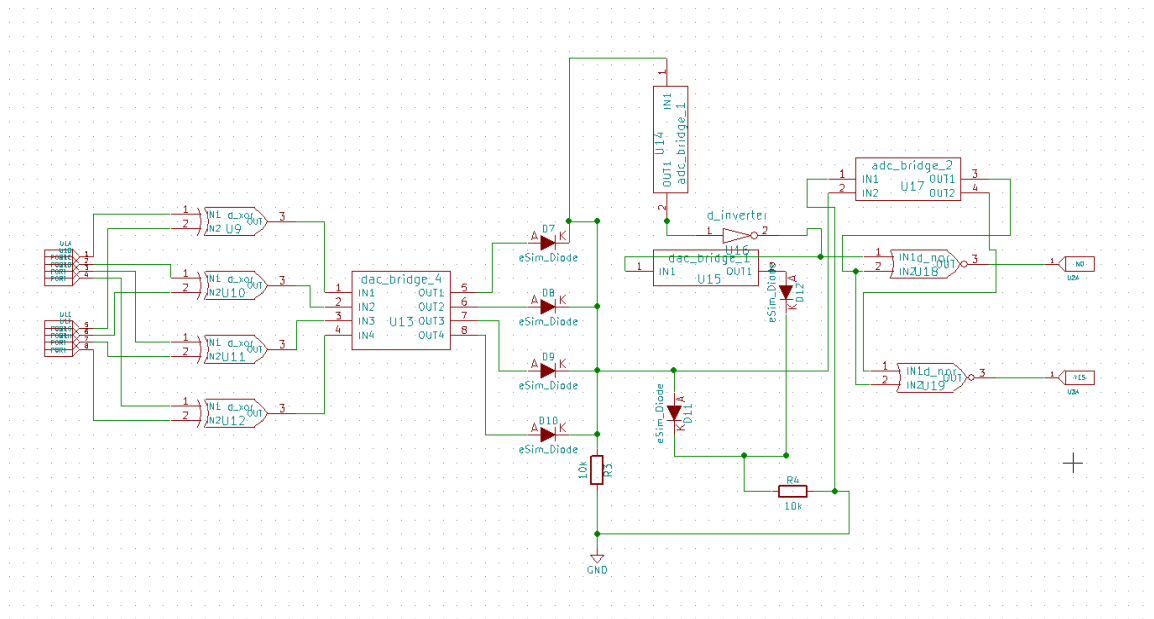
## Circuit Diagrams: -

- This is the main functional circuit schematic of 4-Bit Binary Combinational Lock which uses a subcircuit:



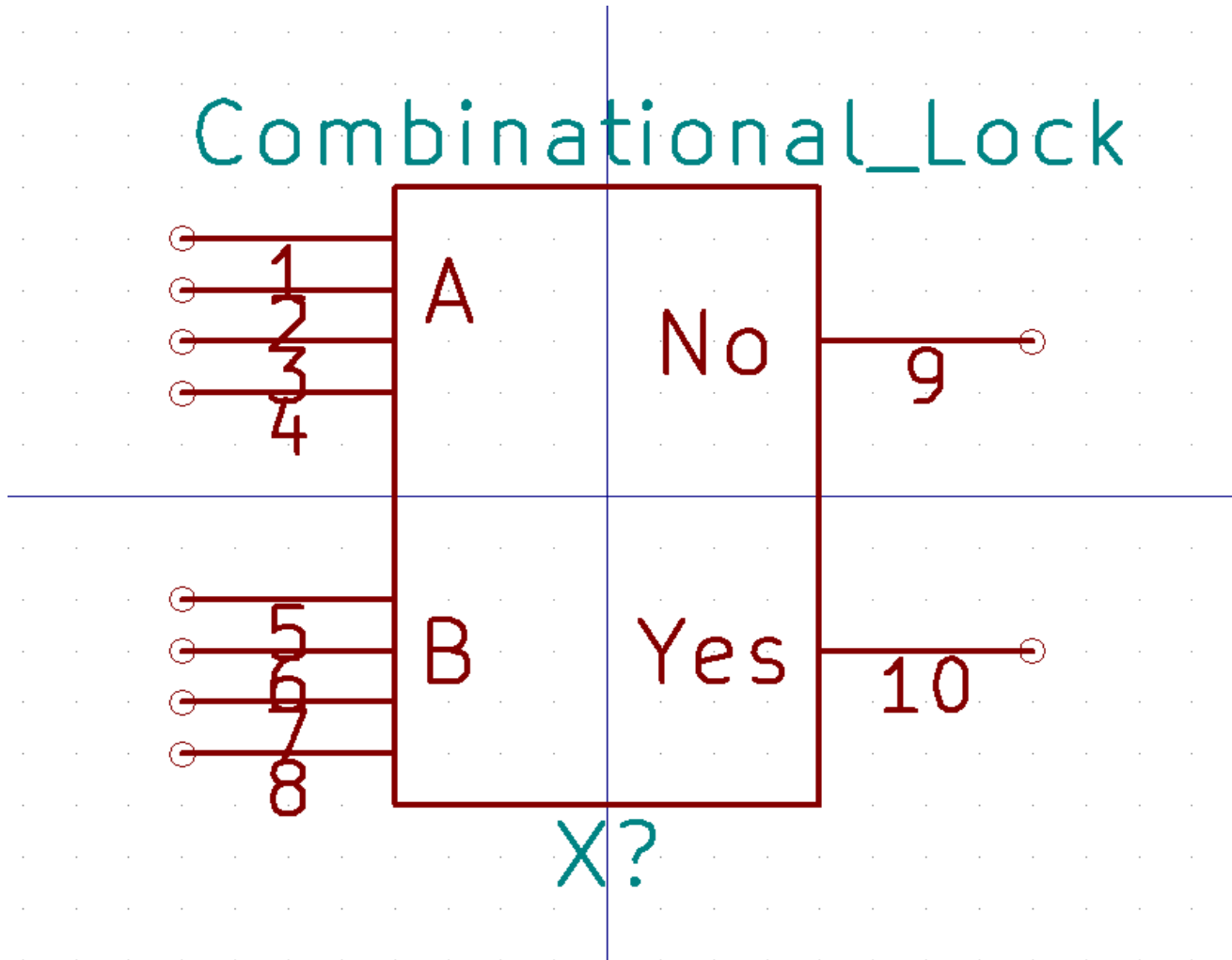
**Main Circuit Schematic – 4-Bit Binary Combinational Lock**

Combinational Lock subcircuit is to check the equality of two 4bit binary digits. The internal structure of the 4-bit Binary Combinational Lock (subcircuit) is shown below:



**Subcircuit Schematic for 4-Bit Binary Combinational Lock**

- The symbol defined/designed to represent the subcircuit is shown below:



Subcircuit Symbol for 4-Bit Binary Combinational Locks

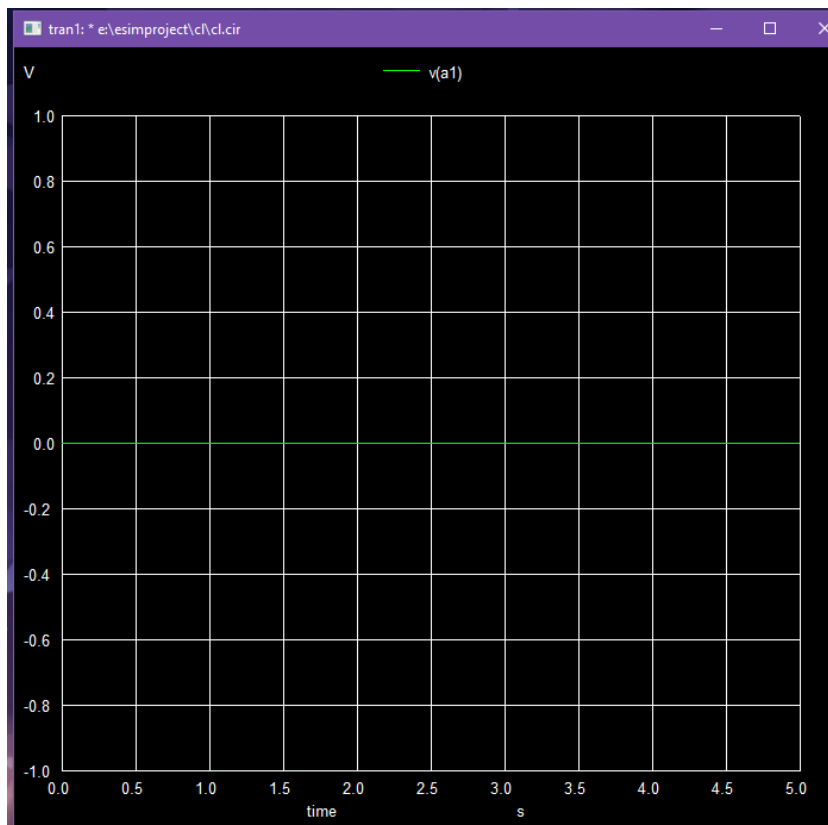
### **Result/Output: -**

### **Equal Combination:**

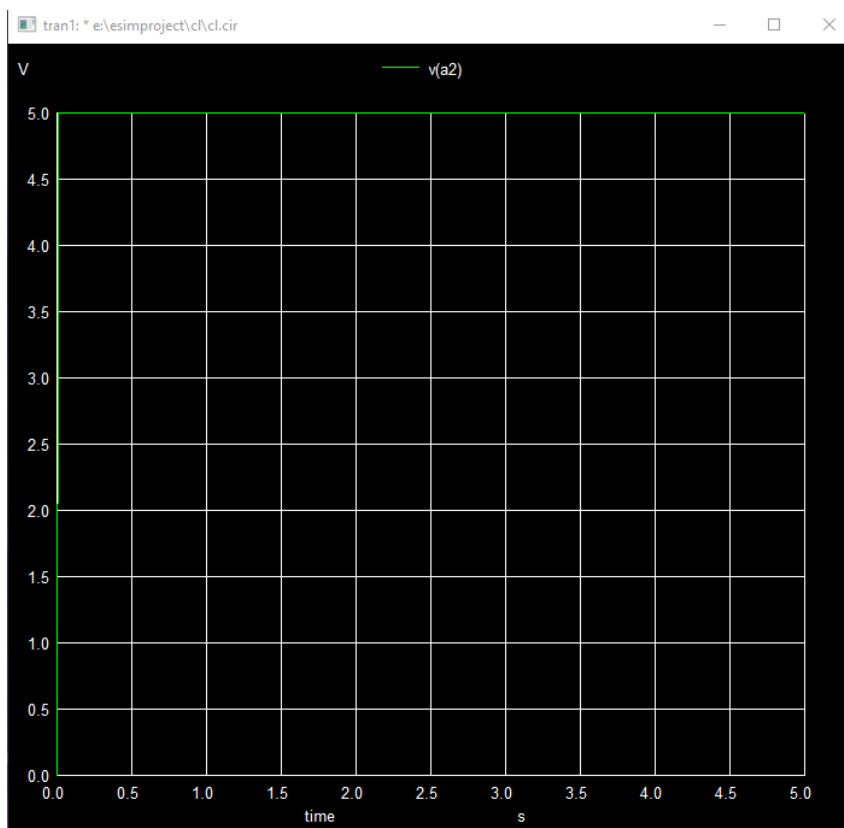
- Ngspice Plots: -**

Inputs: -

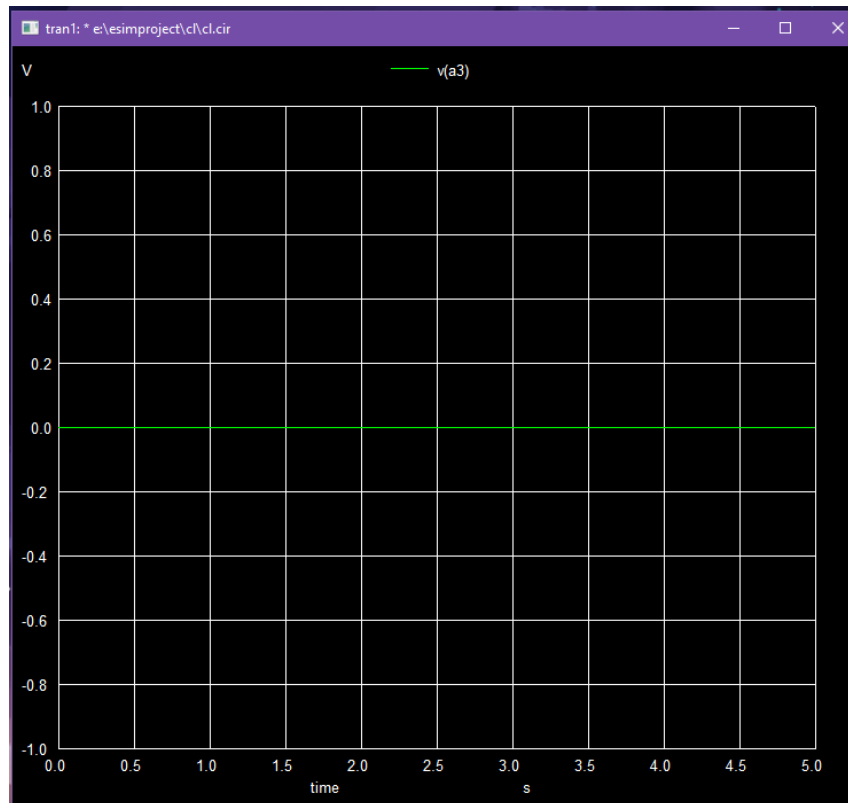
V(A1):



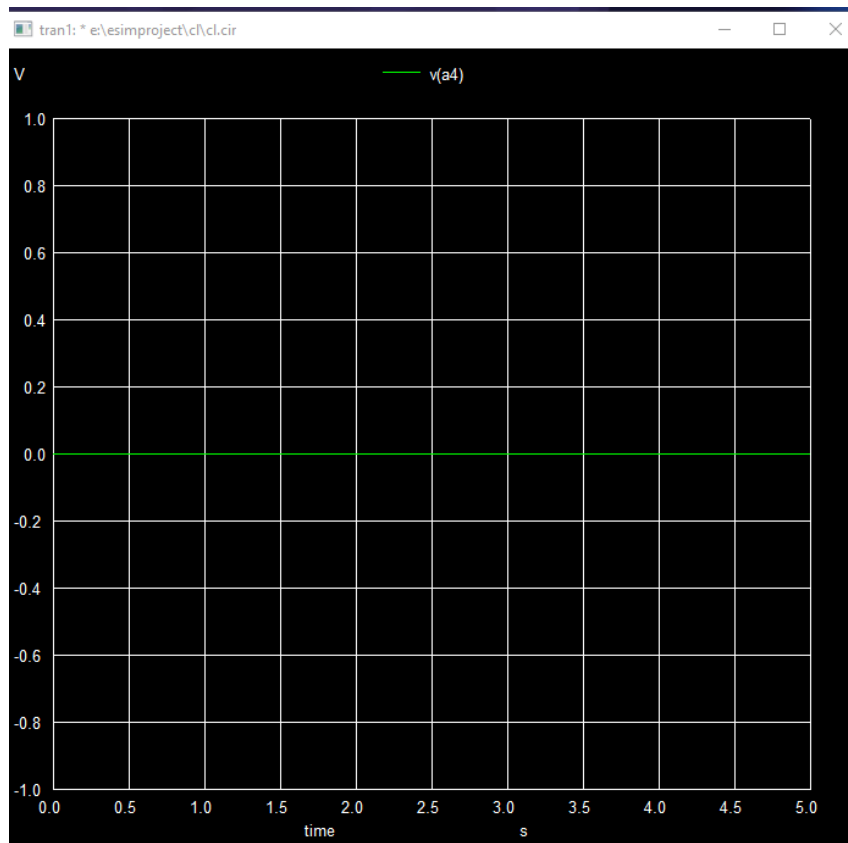
V(A2):



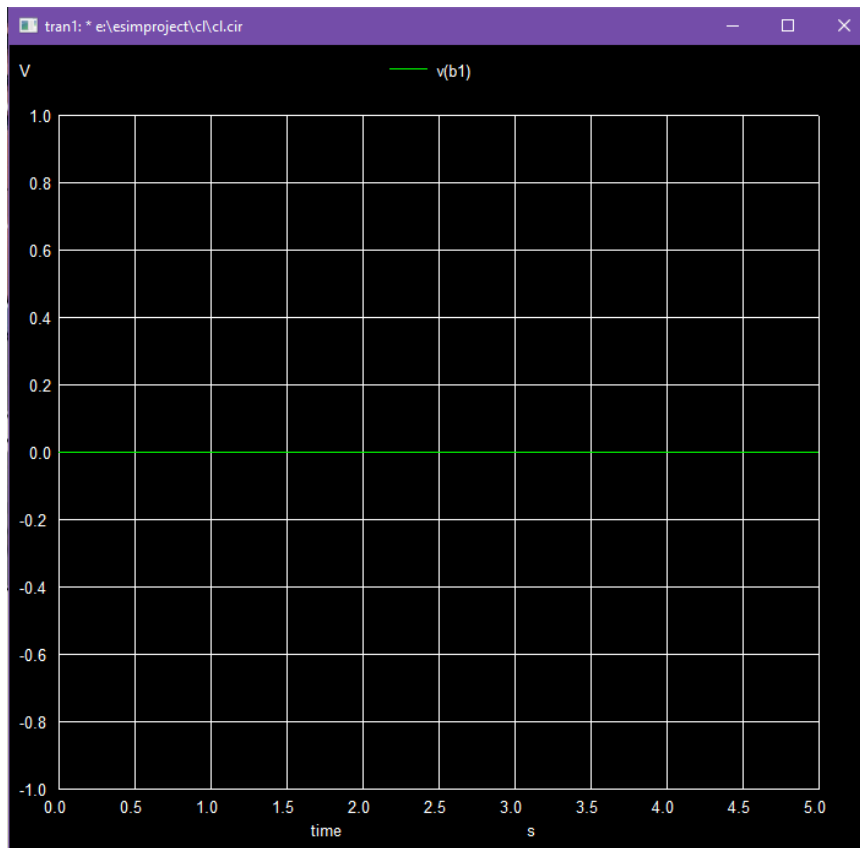
V(A3):



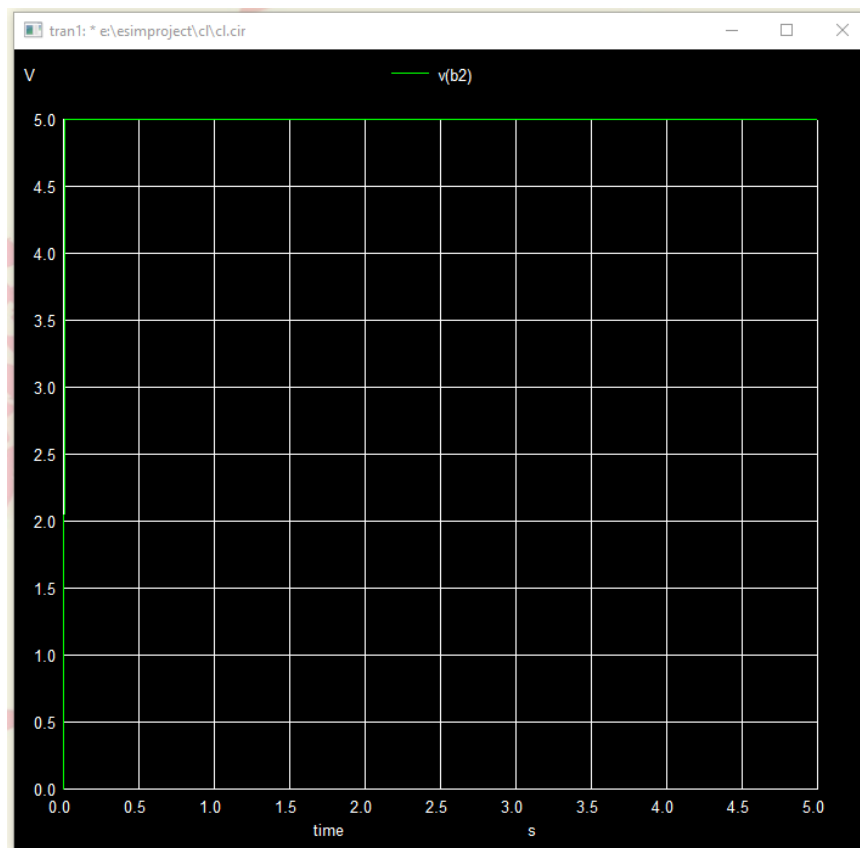
V(A4):



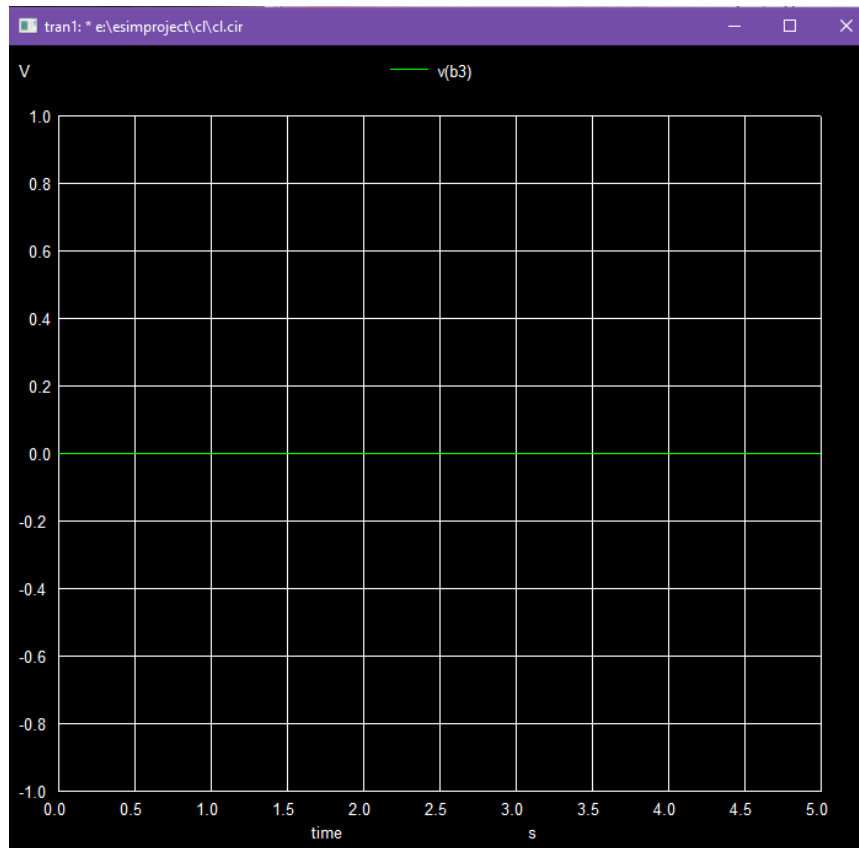
V(B1):



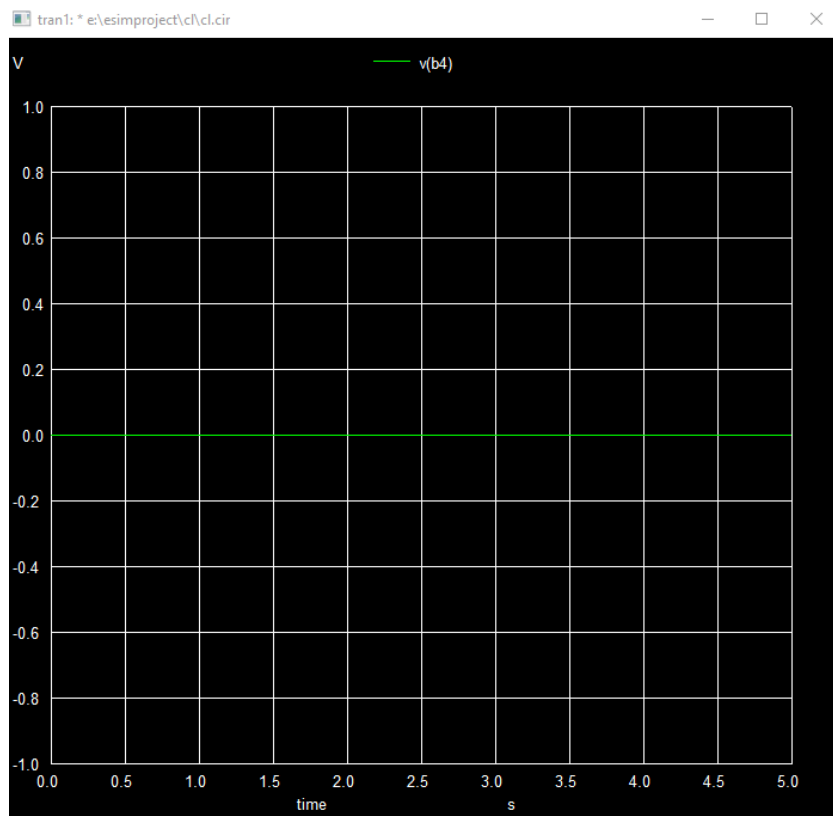
V(B2):



V(B3):

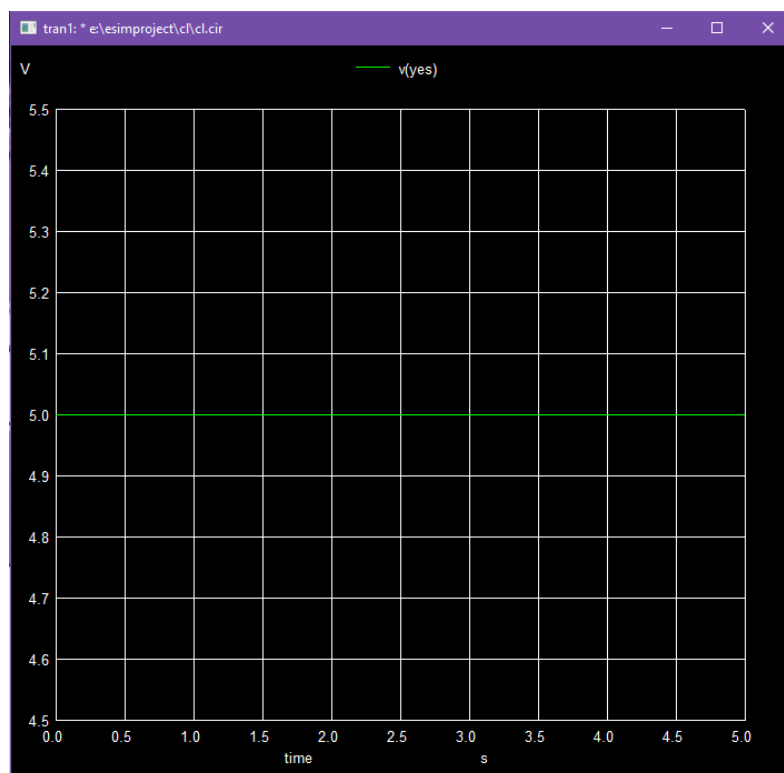


V(B4):

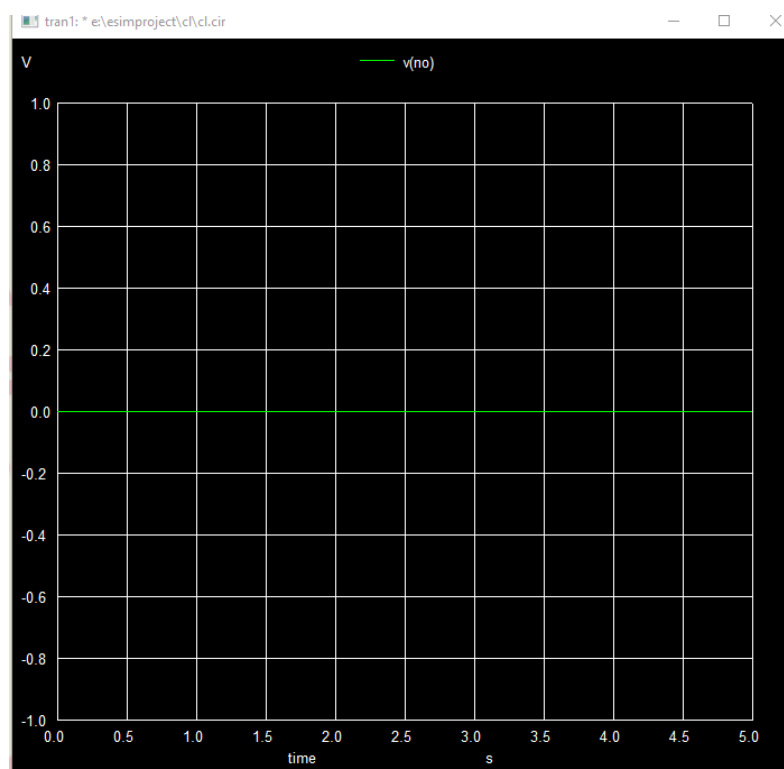


Outputs: -

**V(YES):**



**V(NO):**

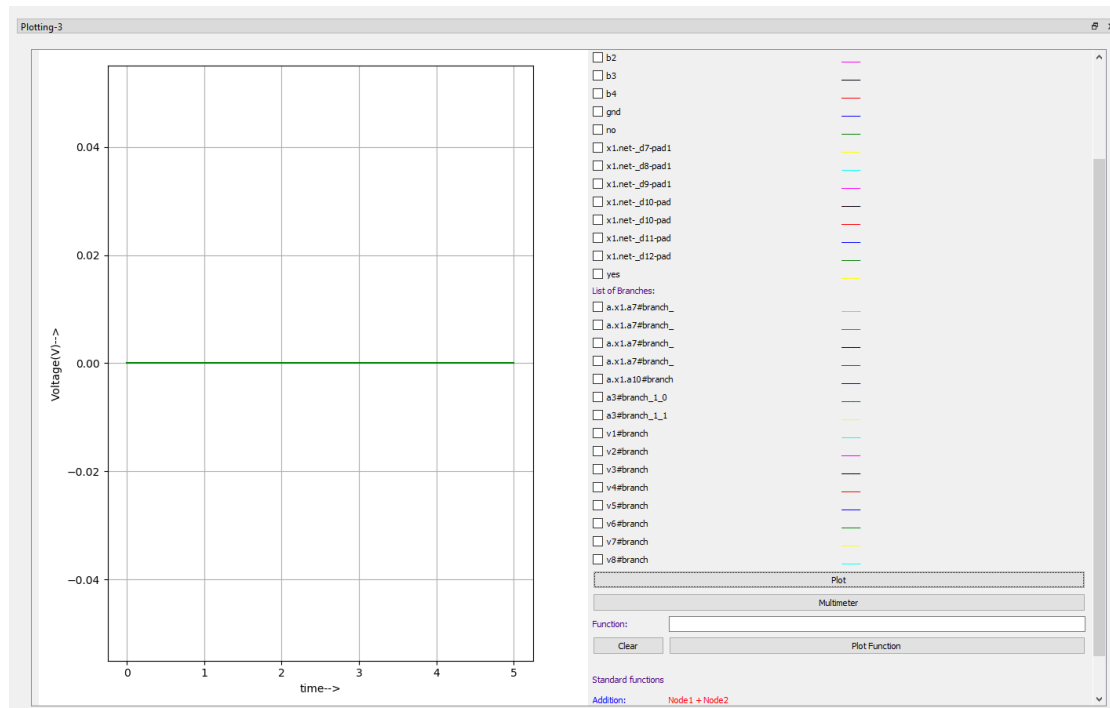




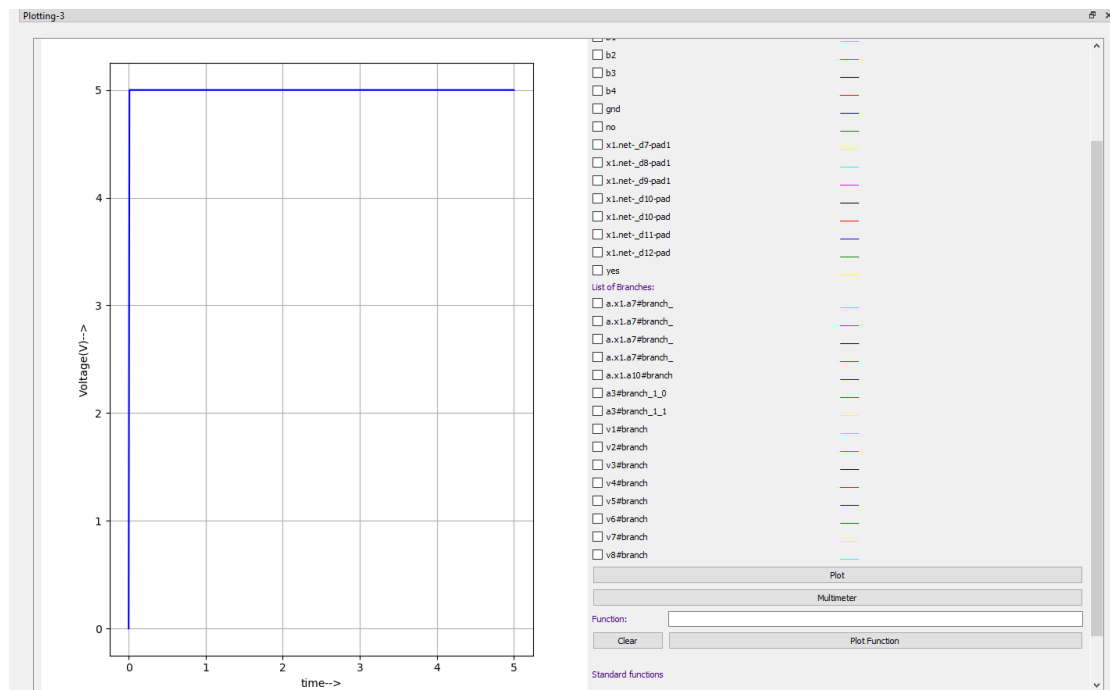
## • Python Plots: - ○

Inputs:

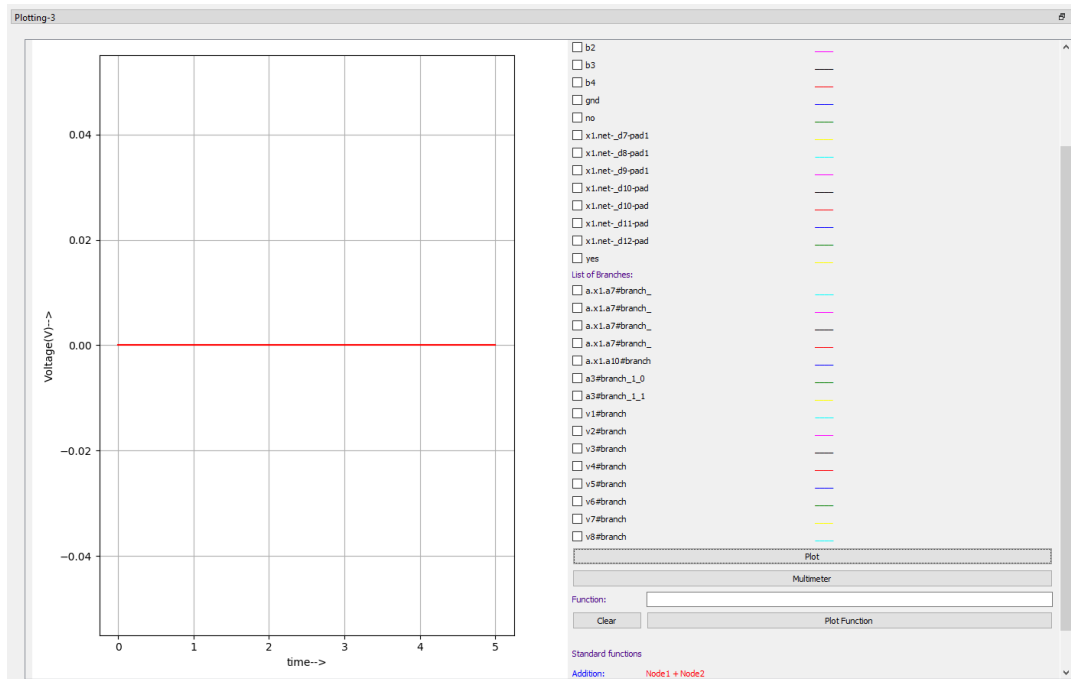
V(A1):



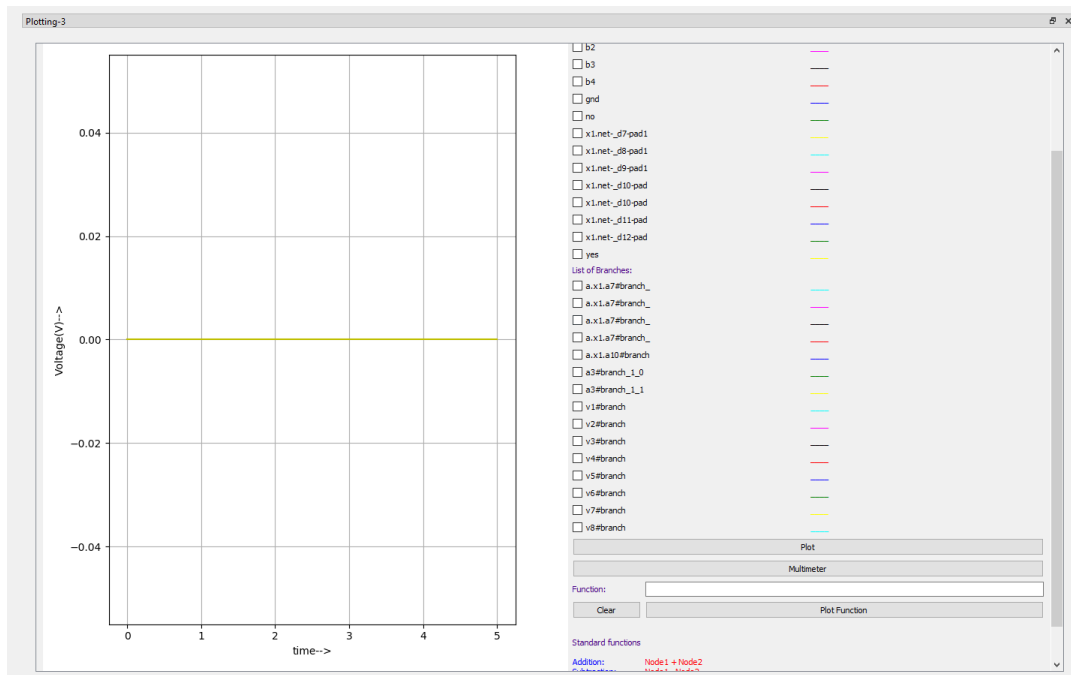
V(A2):



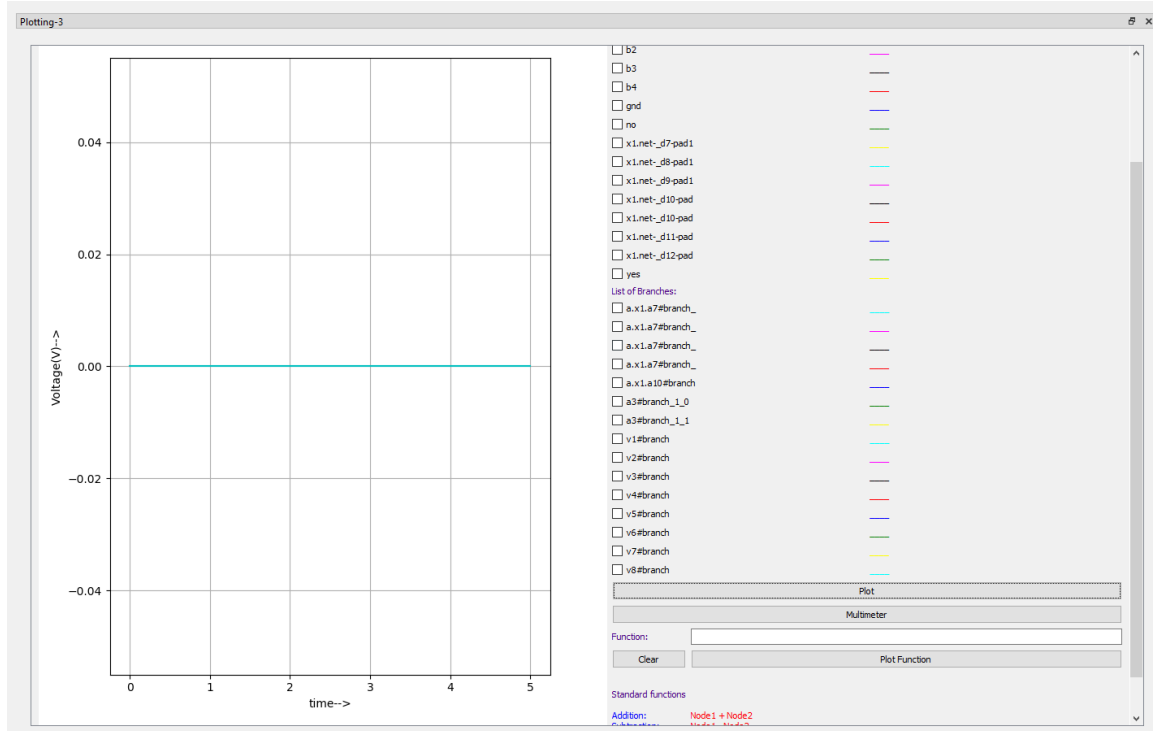
V(A3):



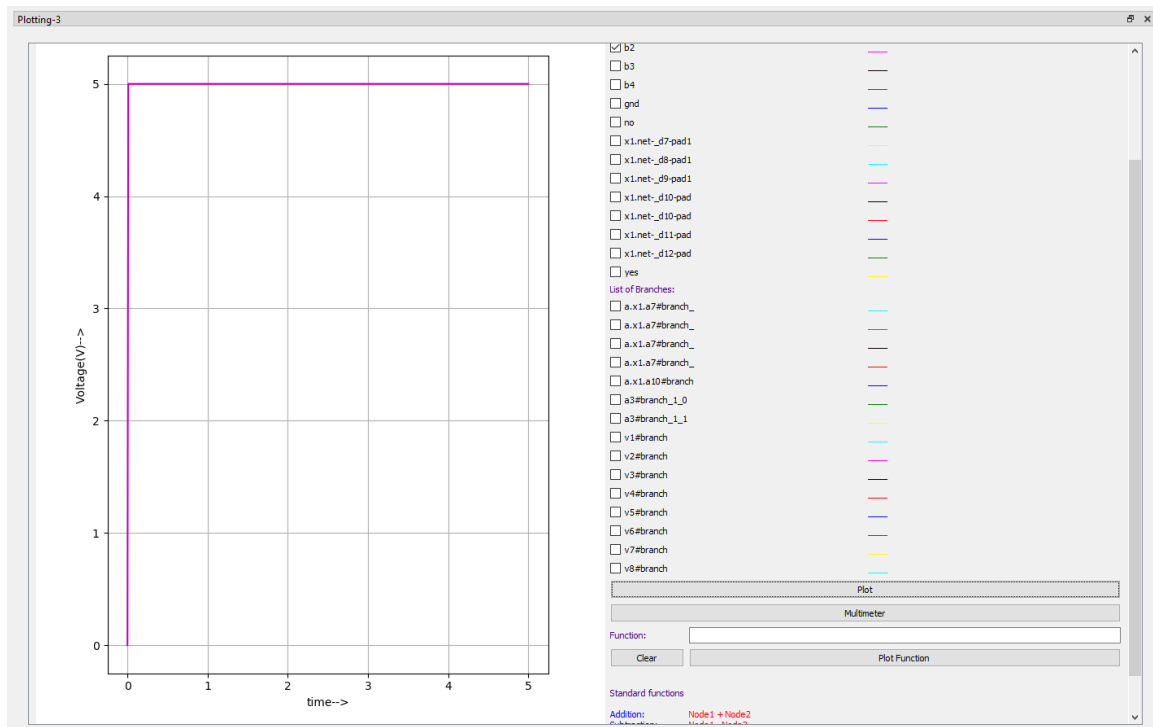
V(A4):



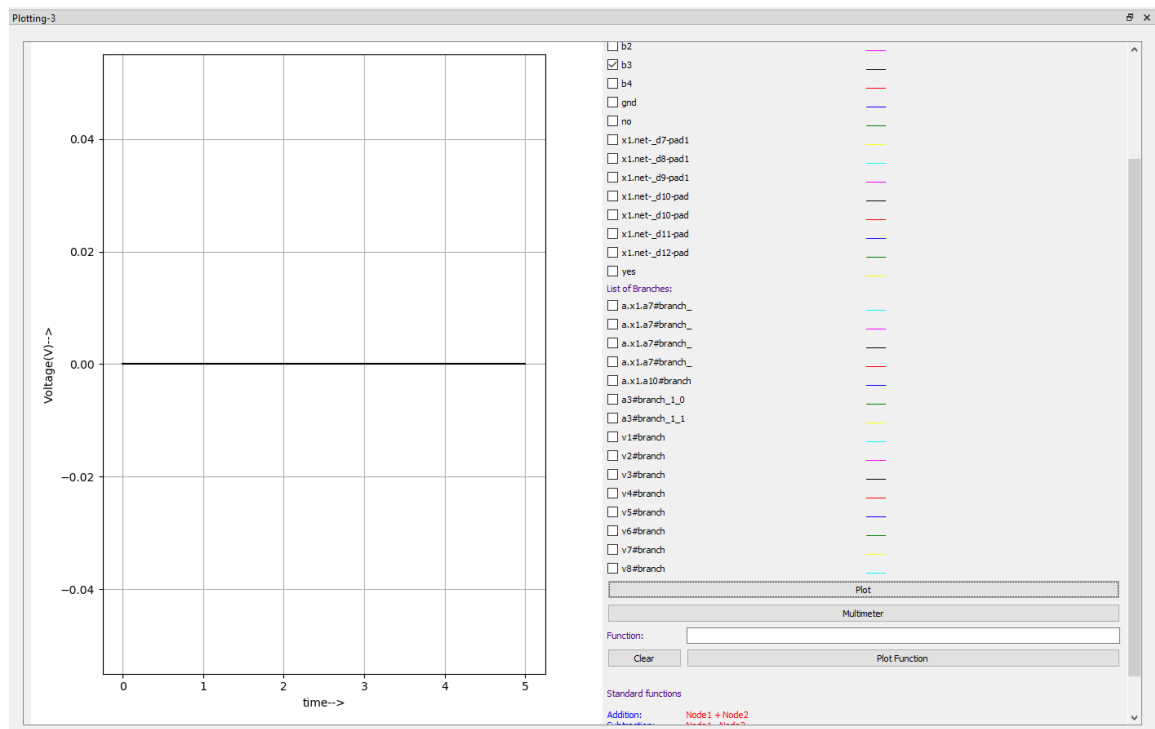
V(B1):



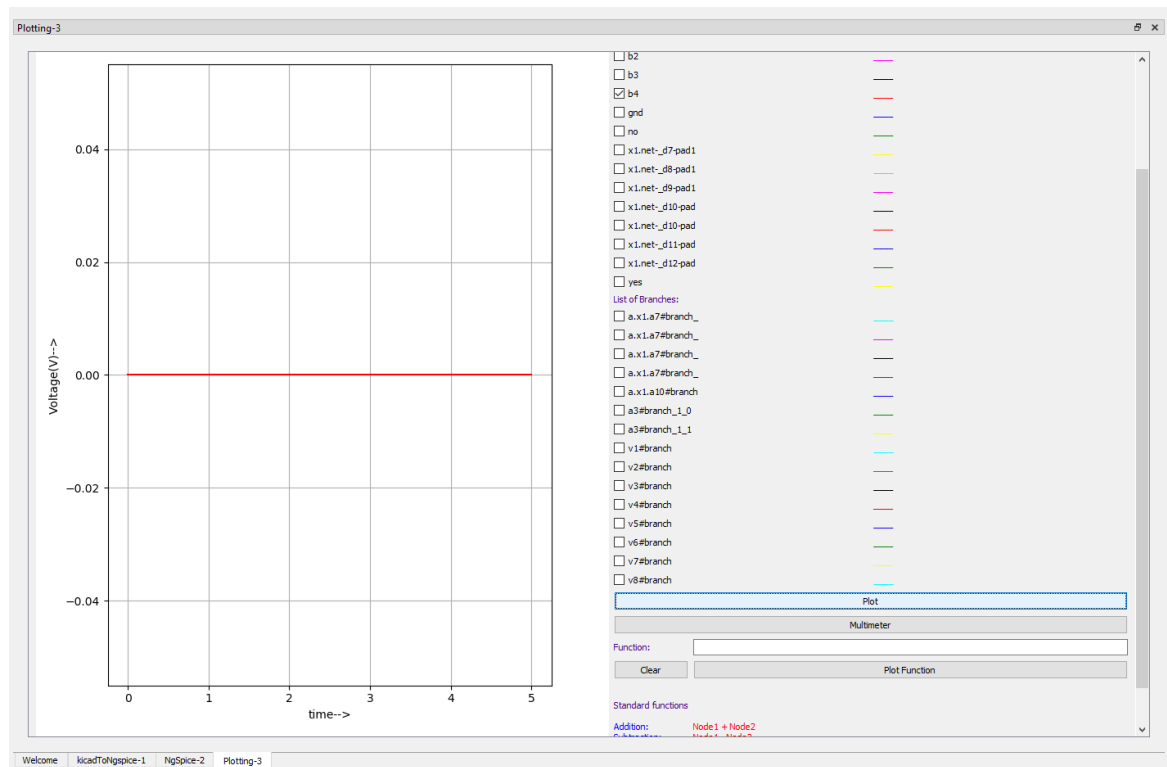
V(B2):



V(B3):

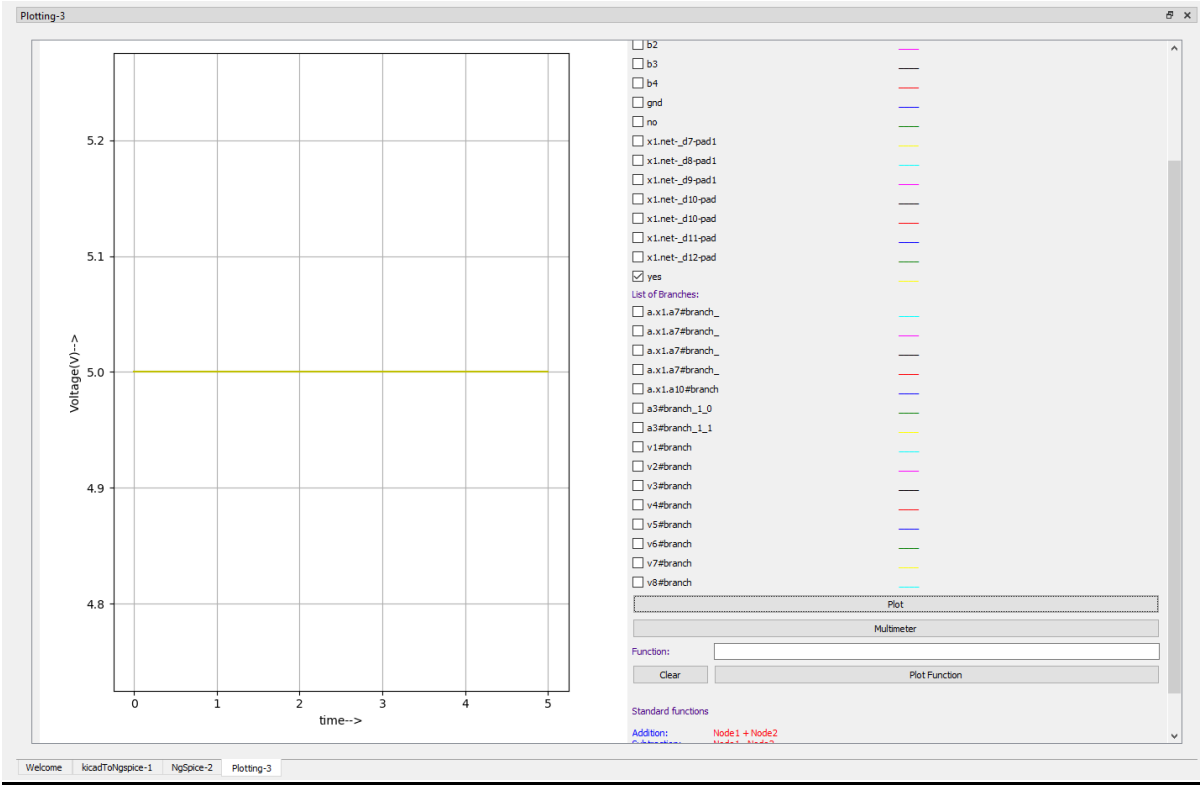


V(B4):

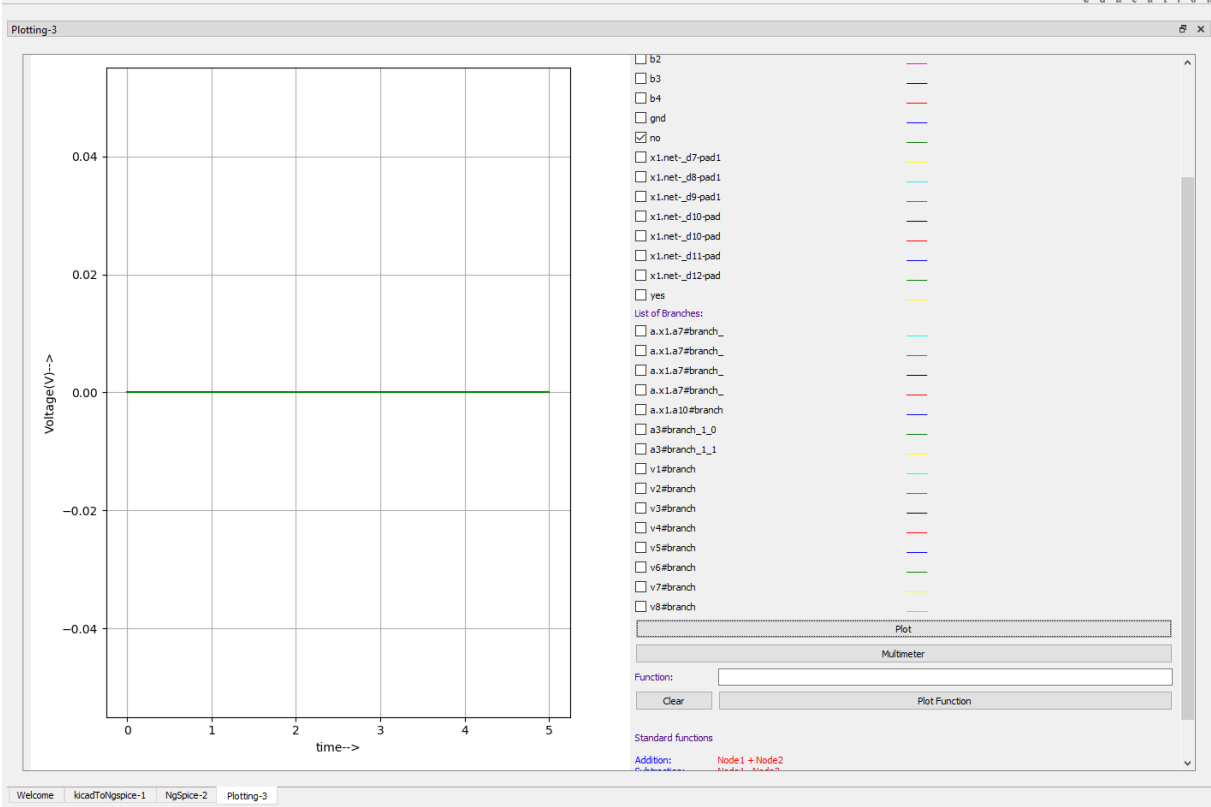


Outputs: -

V(YES):



V(NO):

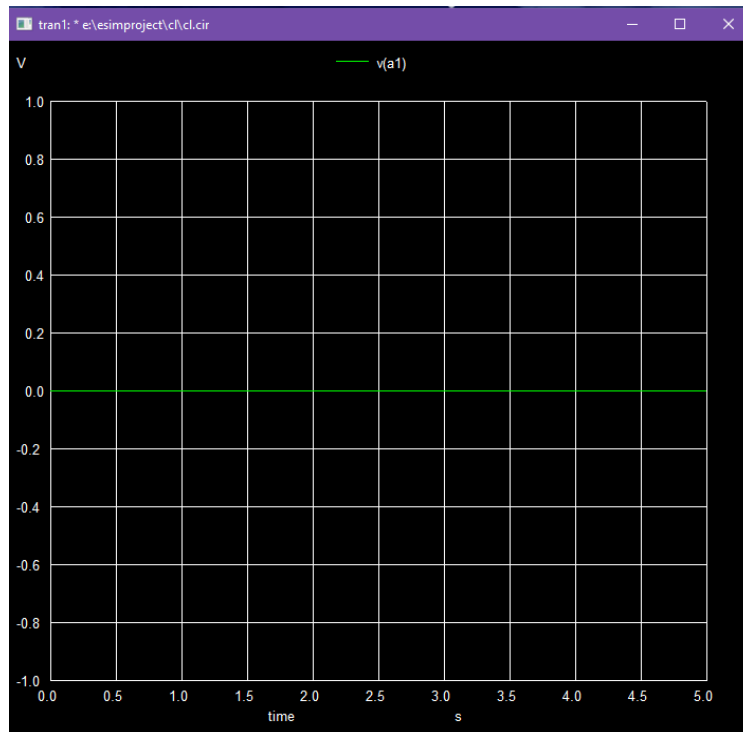


## Unequal Combination:

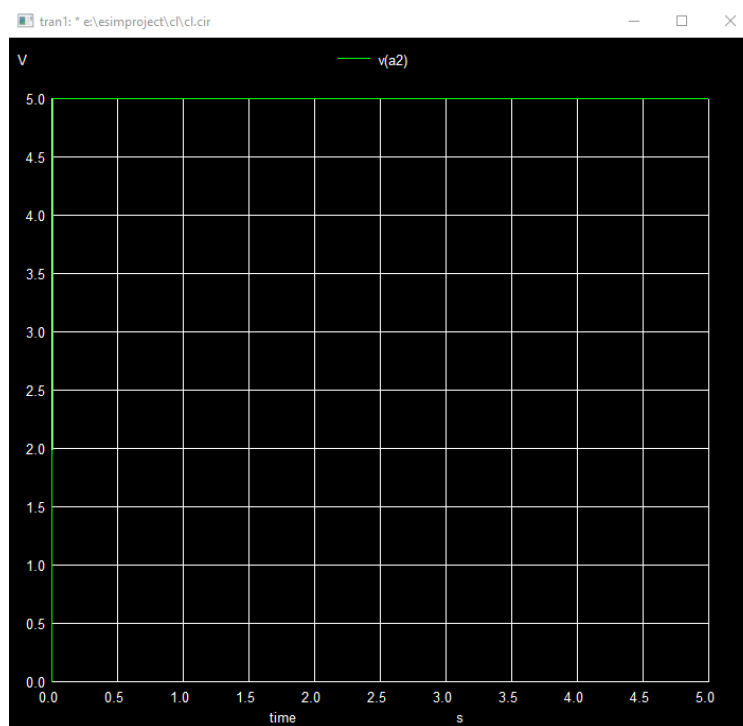
- **Ngspice Plots: -**

Inputs: -

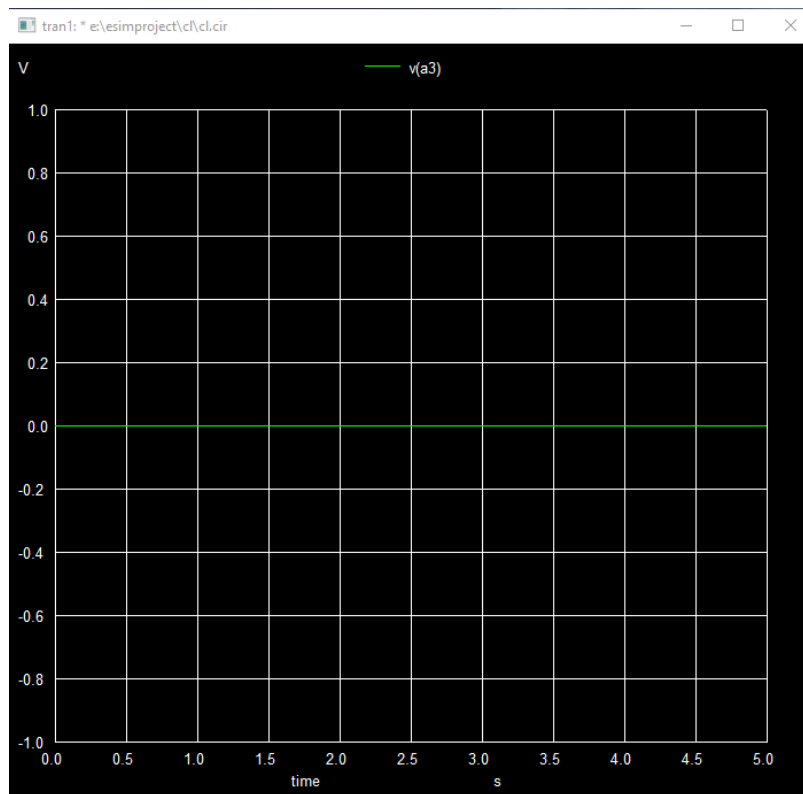
**V(A1):**



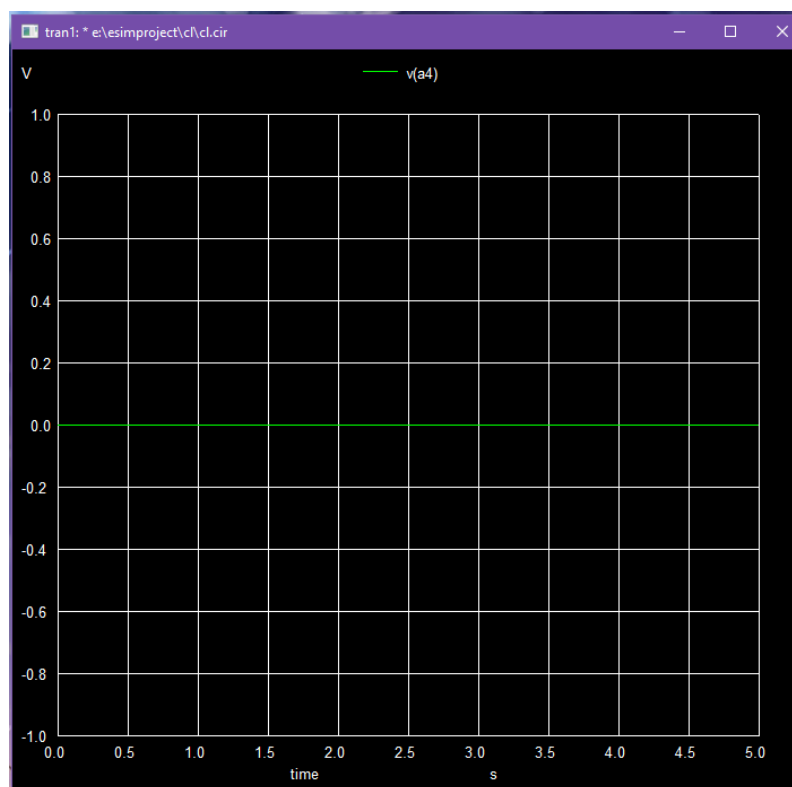
**V(A2):**



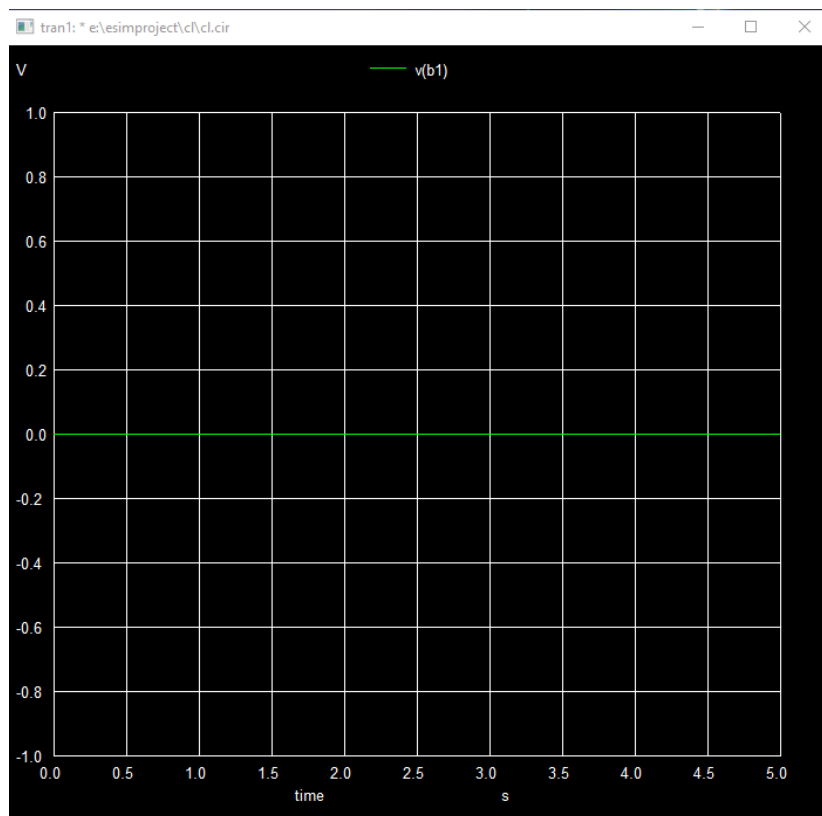
V(A3):



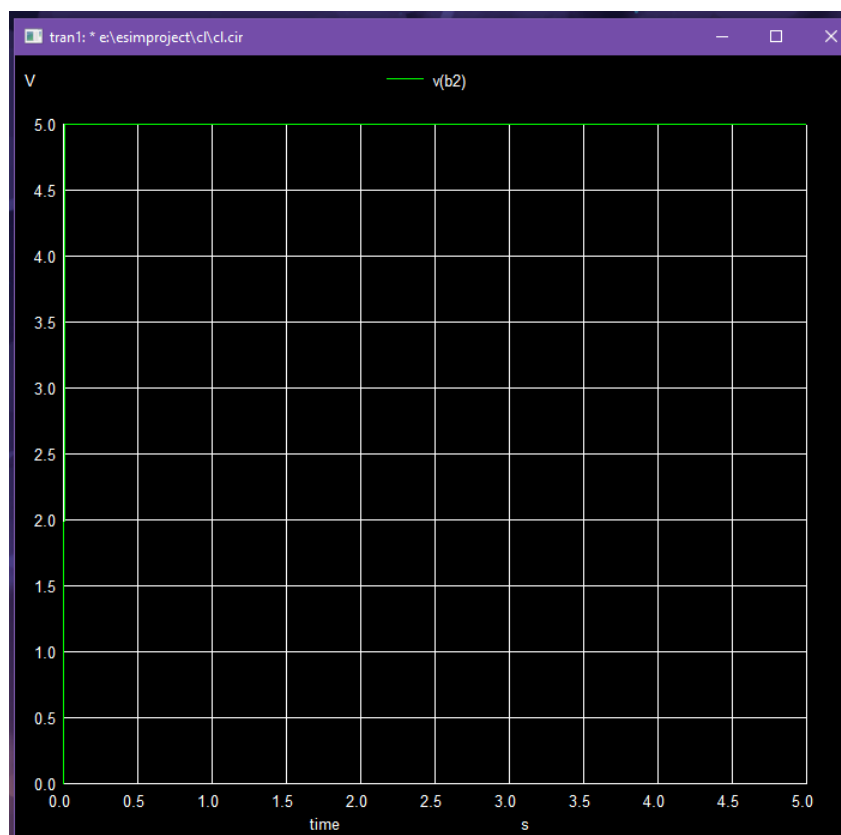
V(A4):



V(B1):

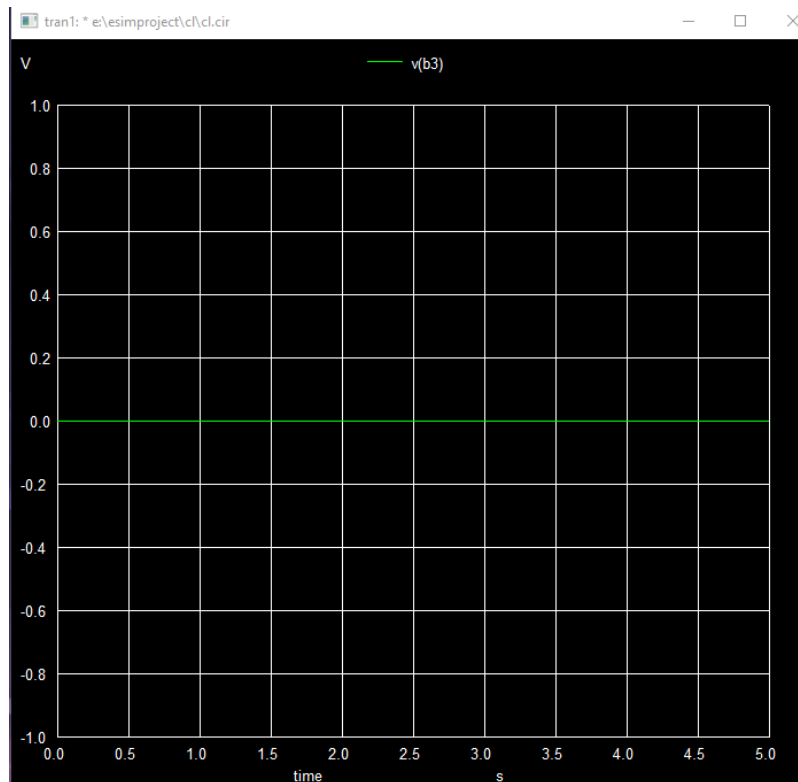


V(B2):

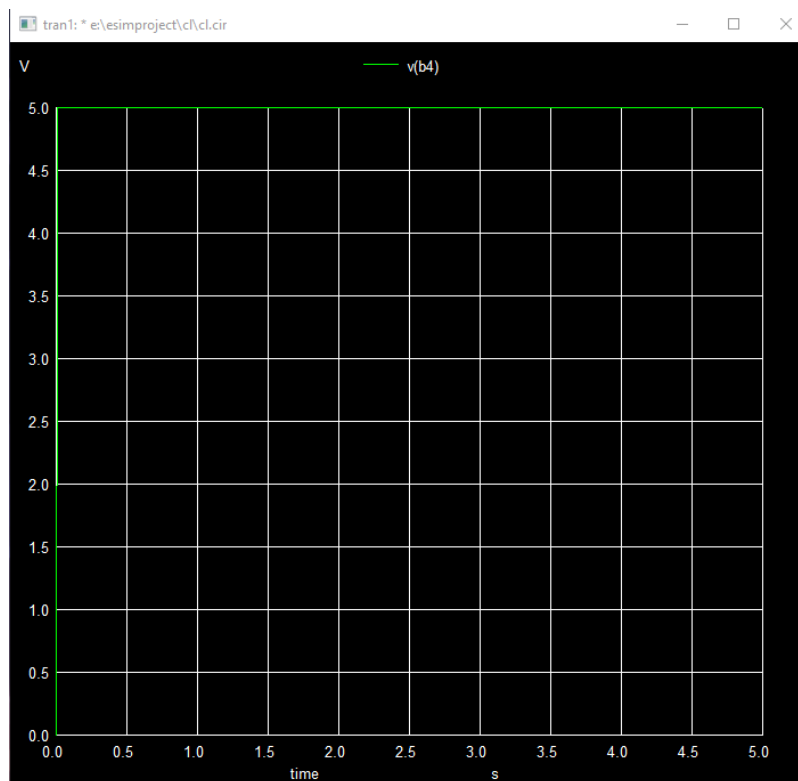




V(B3):

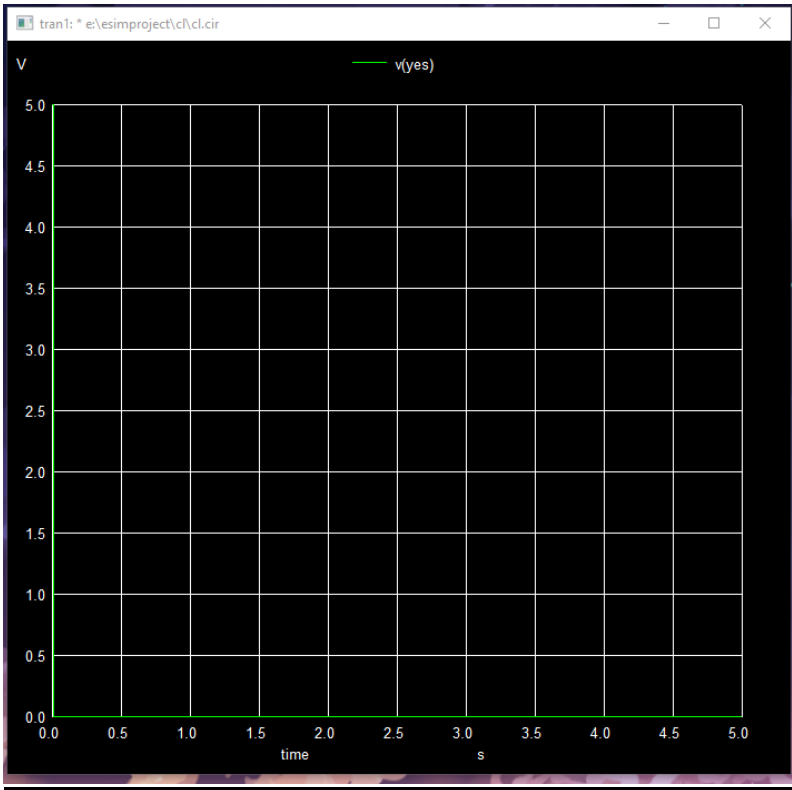


V(B4):

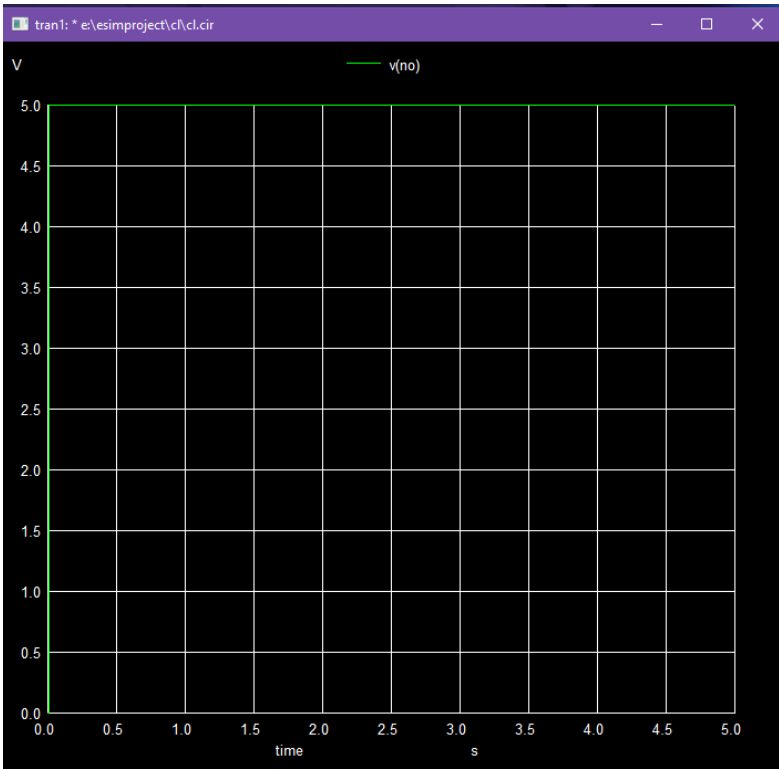


Outputs: -

V(YES):



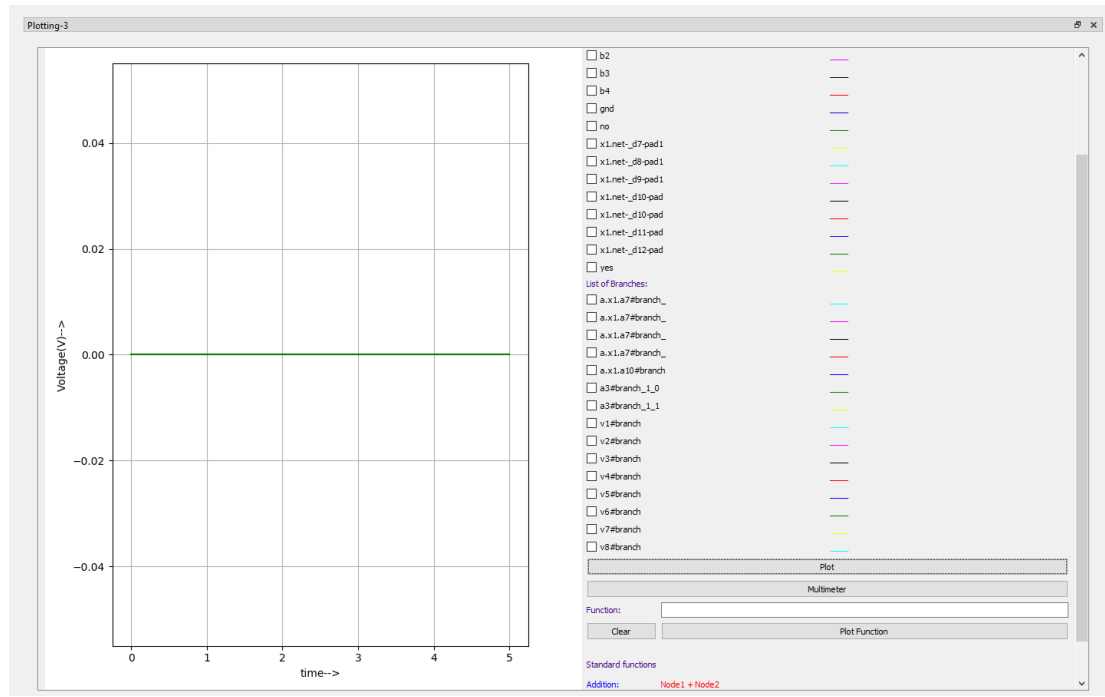
V(NO):



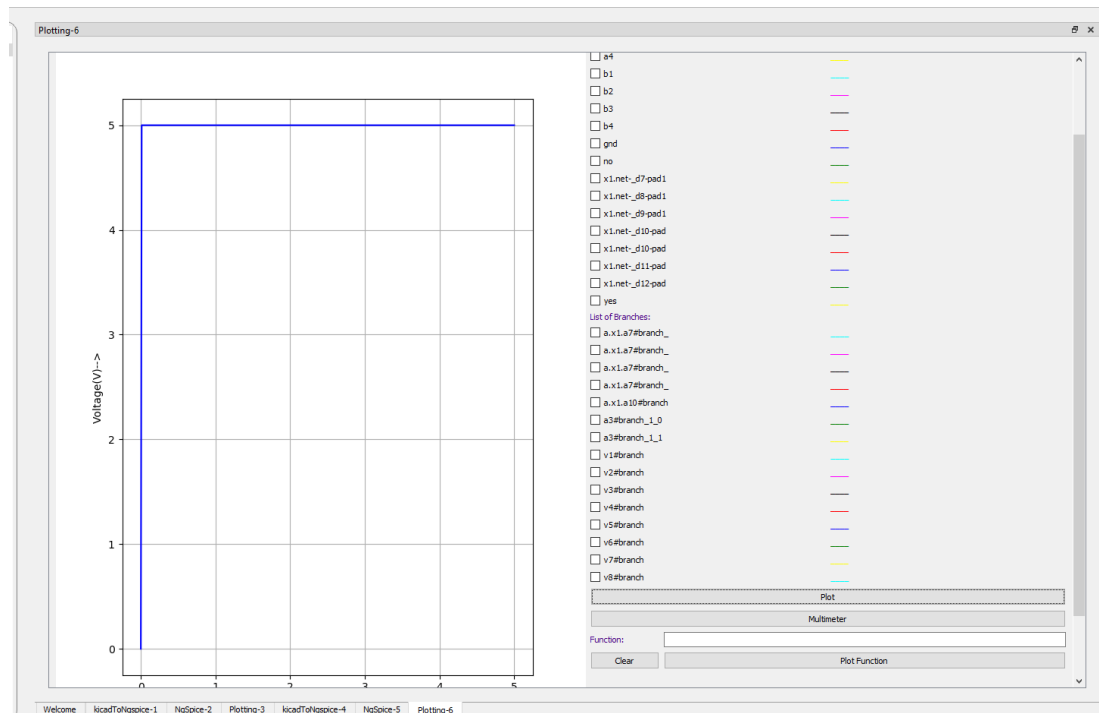
## • Python Plots: - ○

Inputs:

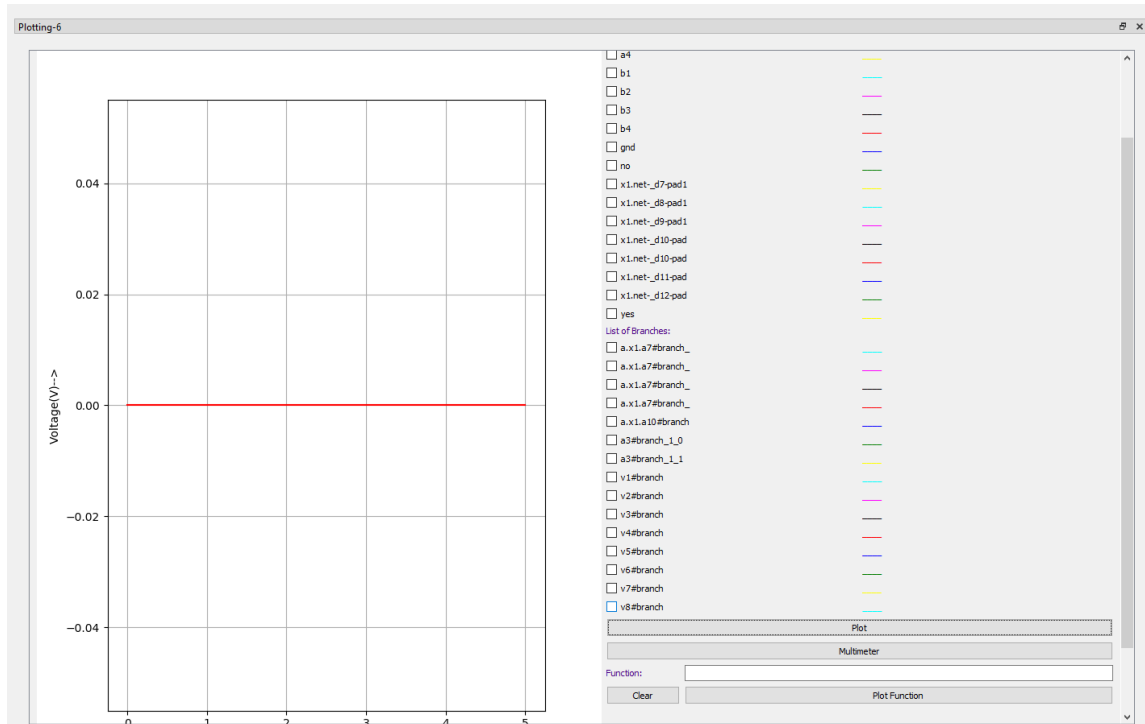
V(A1):



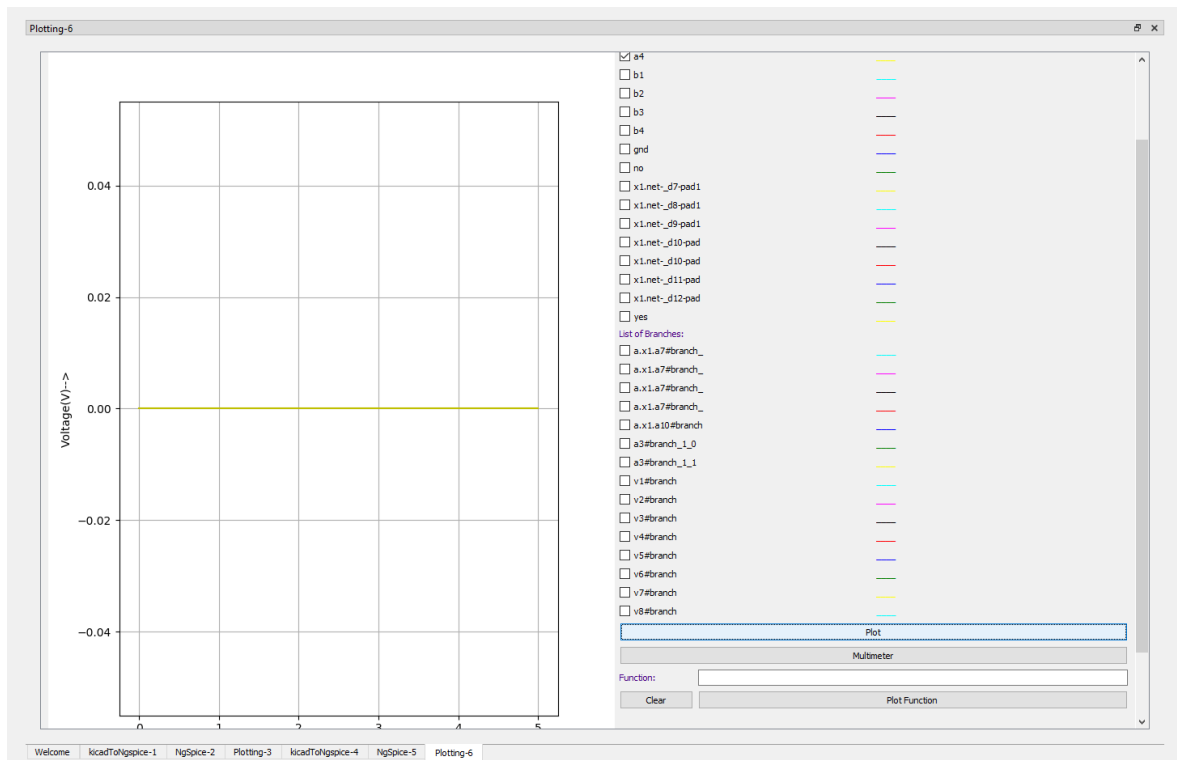
V(A2):



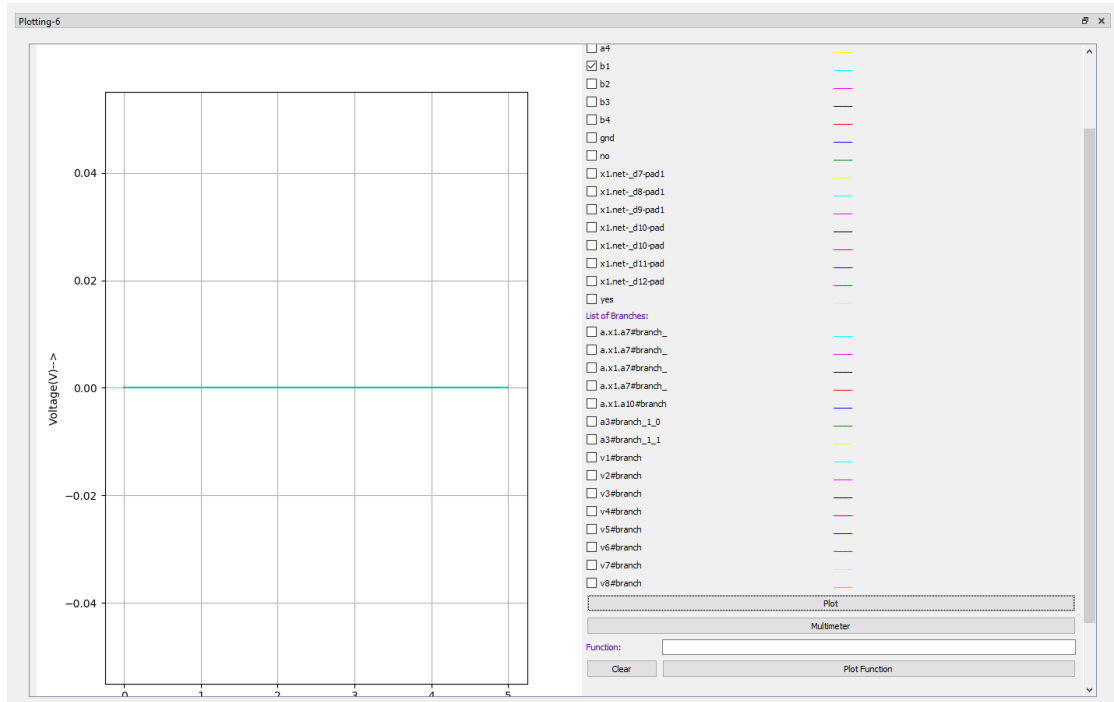
V(A3):



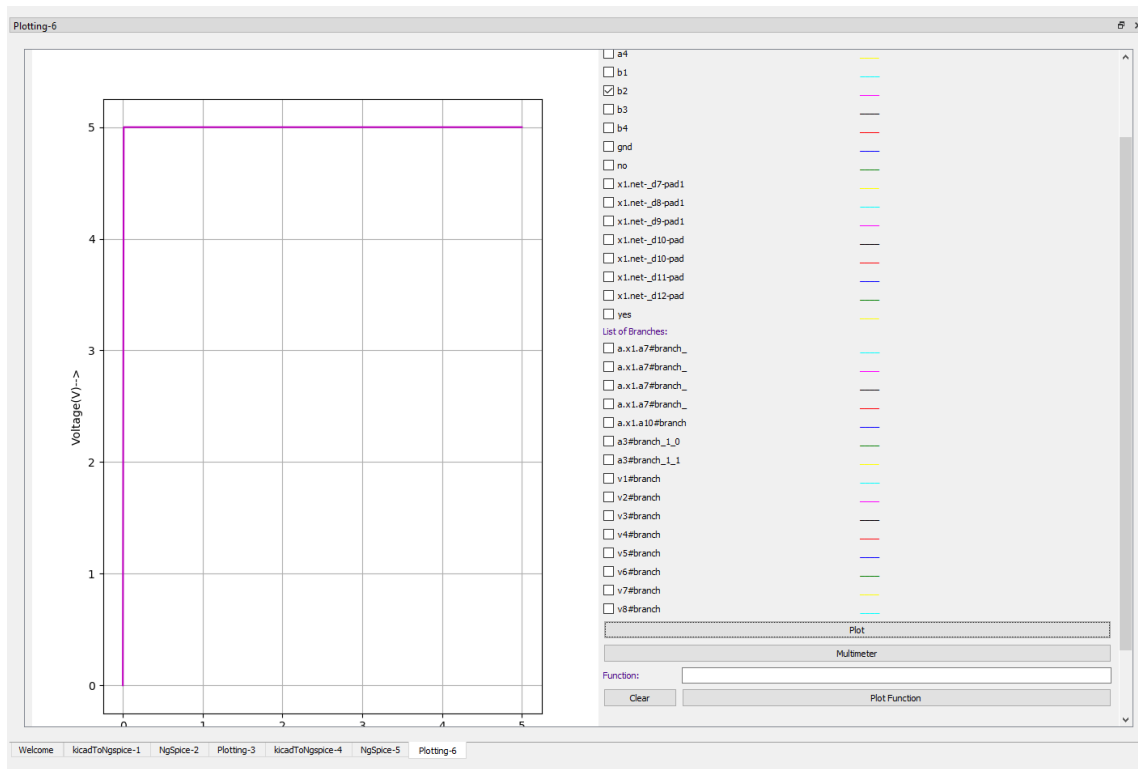
V(A4):



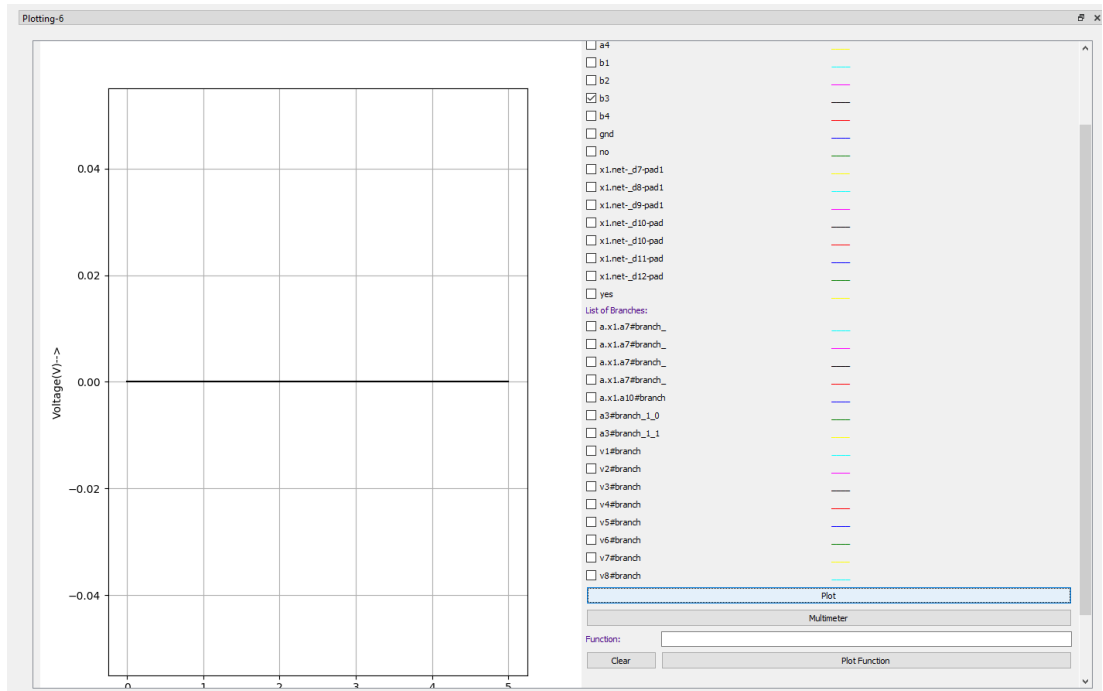
V(B1):



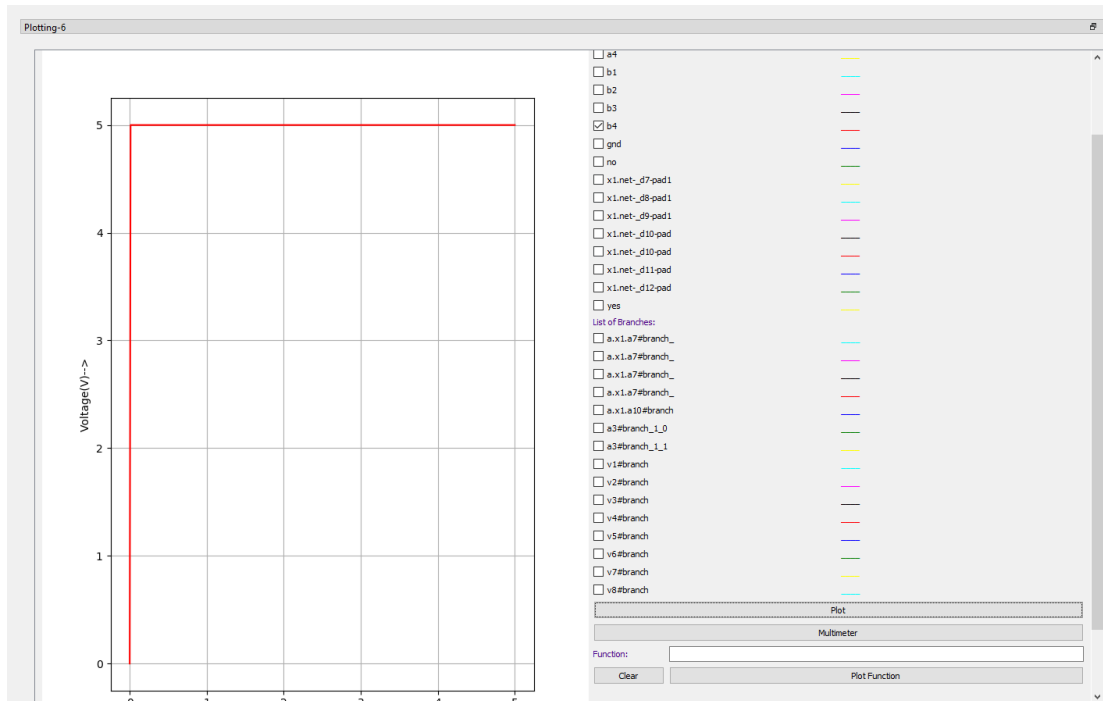
V(B2):



**V(B3):**

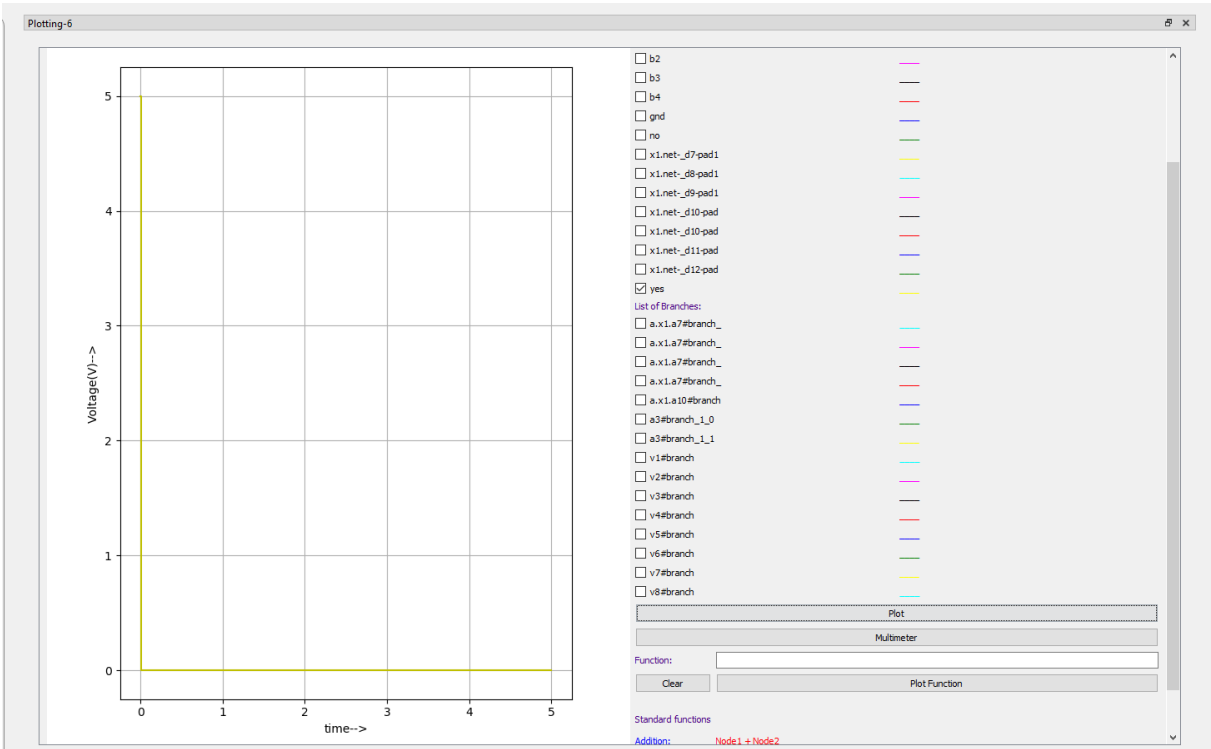


**V(B4):**

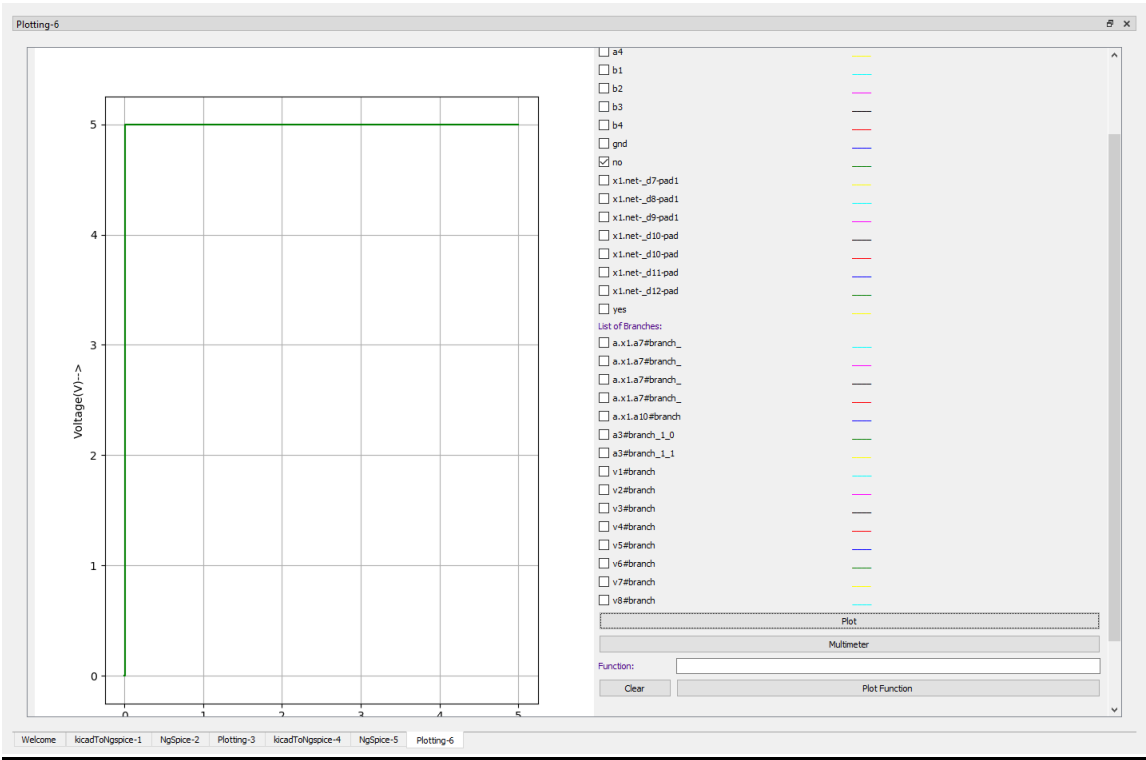


Outputs: -

V(YES):



V(NO):



## **References: -**

- [Simple Combination Lock | Digital Integrated Circuits | Electronics Textbook \(allaboutcircuits.com\)](#)